Topical Workshop on Electronics for Particle Physics

Aix-la Chapelle

September 20-24th 2010

LPNHE Paris, October 2010

Jean-Francois Genat

http://indico.cern.ch/...

Program

Plenary talks

HEP in Germany	Bernhard Spaan	(TU Dortmund)
Advanced Electronics for HEP and beyond…	Karlheinz Meier	(U Heidelberg)
HEP at Aachen	Lutz Feld	(U Aachen)
Electronics for FEL, a high rate camera	Peter Goettlicher	(DESY)
LHC Status and Plans	Ralph Assmann	(CERN)
ASICs and FPGA at ESA	Roland Weigand	(ESA)
3D MPW runs for HEP	Kholdoun Torki	(CMP Grenoble)
Optical Technologies for Data Communications	Francois Vasey	(CERN)
New interconnect technologies	Piet de Moor	(IMEC)
Preparation for heavy ions at ALICE and other LHC experiments	Andrea Dainese	(INFN Padova)
Obsolescence issues for the LHC Electronics	Vincent Spellane	(Lockeed Martin)
Physics for pedestrians	Patrick Puzo	(LAL Orsay)

Working Groups

Power	Philippe Farthouat	(CERN)
Microelectronics Users Group	Kostas Kloukinas	(CERN)
Opto Working Groups	K.K. Gan	(Ohio state U)
xTCA	Magnus Hansen	(CERN)

Program

Parallel Sessions

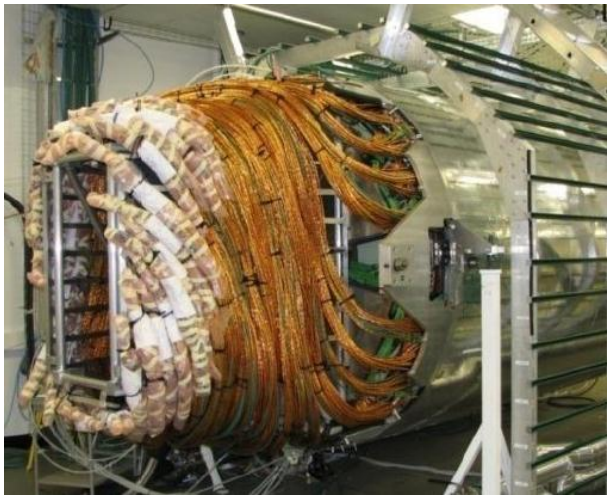
ASICs (Three sessions)
Opto and Links
Power, Grounding & Shielding
Data Acquisition, xTCA
Packaging and Interconnect
Triggers
FPGA
Radiation hard devices
Status reports
LHC under first beam conditions

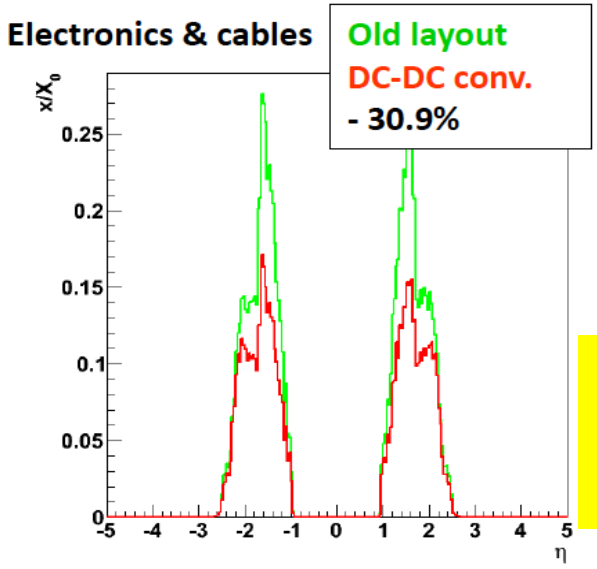
150 Posters…

Outline

Power
DC-DC Converters vs Serial

DC-DC Powering CMS Tracker (Aachen)

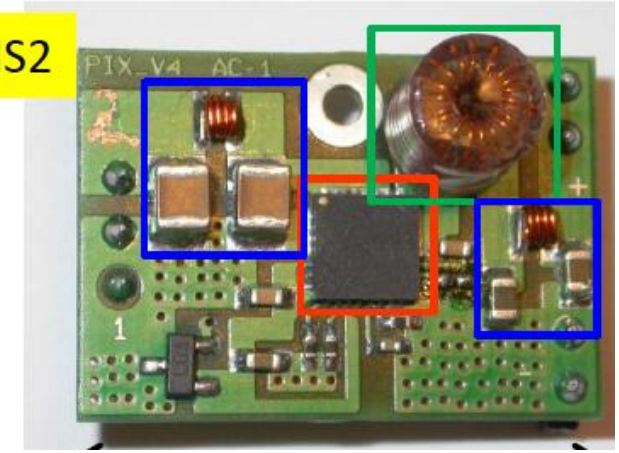




Higher V lower I
Less Joule… (ndr)

TWEPP 2010 :
Katja Klein (Aachen)
Jan Sammet (Aachen)

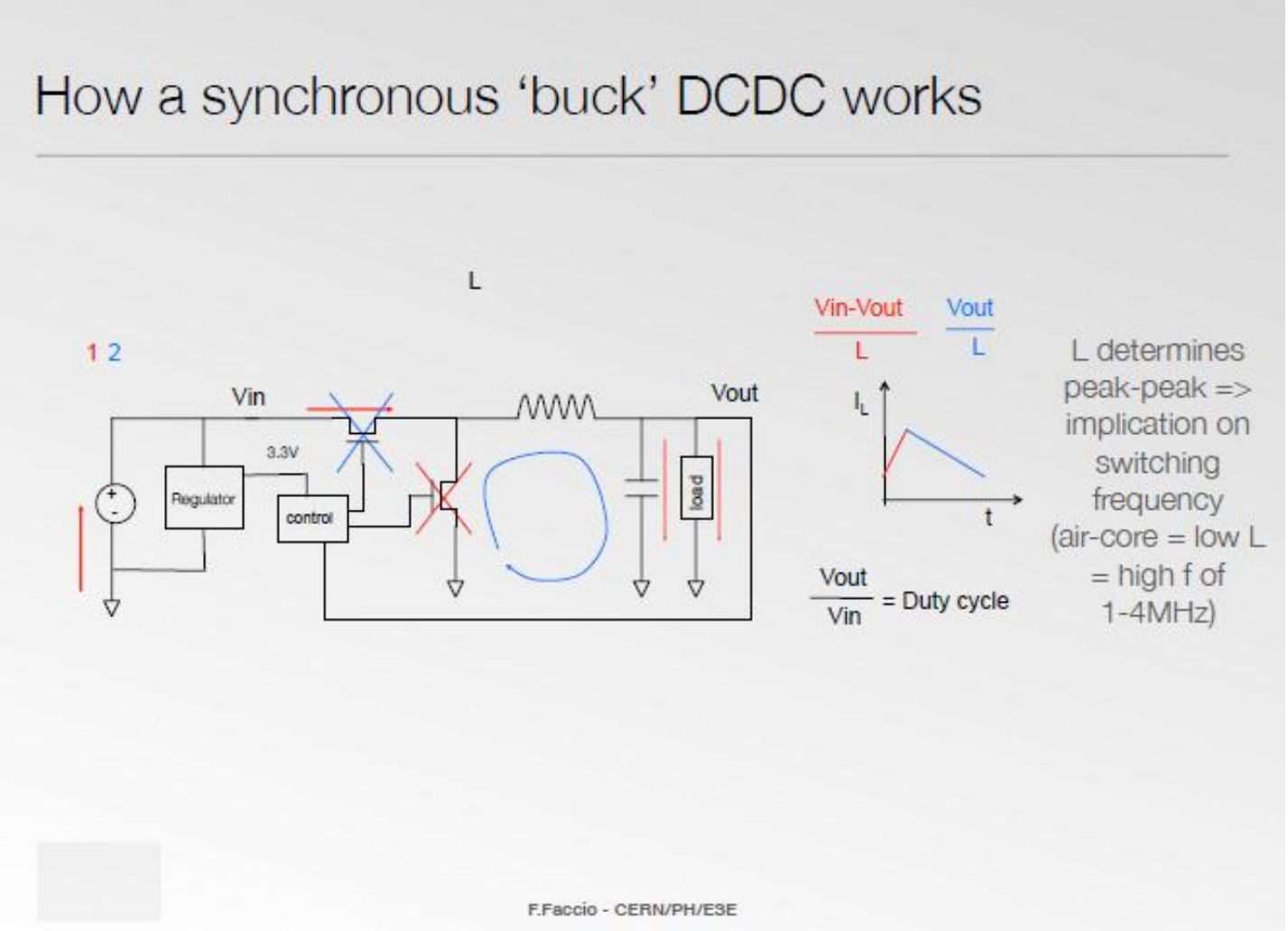
AMIS2



Radhard (MGy) AMIS2 Chip by CERN
DC-DC System with aircore coil (4T CMS field)

V_{in} = 3-12 V
I_{out} < 3A
V_{out} = 1.2, 2.2, 3.3 V
f_s = 600 kHz – 4MHz

DC to DC ASIC



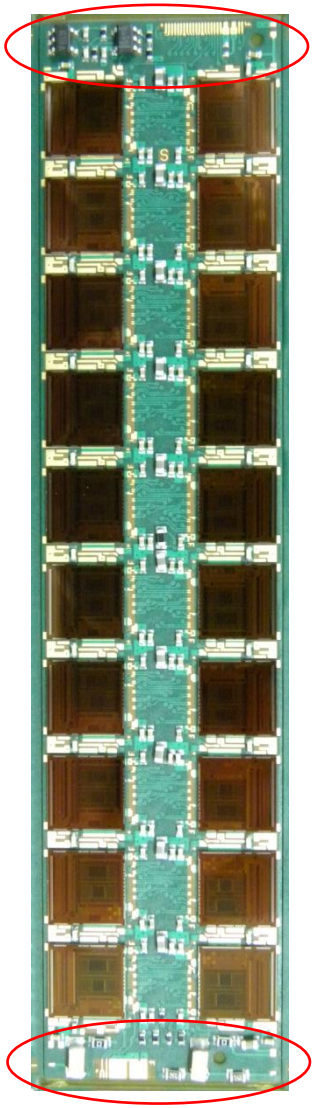
ASIC: Latchup and Radiation Hardness problems (ndr)

Federico Faccio (CERN)

Silicon strips for the ATLAS upgrade

Stave Hybrid – Layout and Electrical Detail

- Hybrid is designed to accommodate 20 x ABCN-25 readout ASICs (2 columns of 10)
- Layout topology matches ATLAS07 large area sensor and serially powered Bus cable
  - ASICs placed to match sensor pitch and bond pad profile
  - Hybrid Power and Digital I/O bond fields at opposite ends
- Circuit exploits features of ABCN-25
  - Bi-directional data paths
  - Embedded distributed shunt regulators (for serial powering)
    - Requires external control circuit



Mshunt control and Digital I/O

Hybrid Power and sensor HV filtering (spec'd to 500V)

Pixels

ATLAS Pixels

Frontend FE-I4 for ATLAS pixel detector upgrades
IBL Project (2014) and sLHC
Common design effort: Bonn, CPPM, Genua, LBNL, NIKHEF

- Rad.-hardness >200 MRad TID (FE-I3: >50 Mrad)
- ToT coded in 4 bits.
- detector leakage current > 100 nA

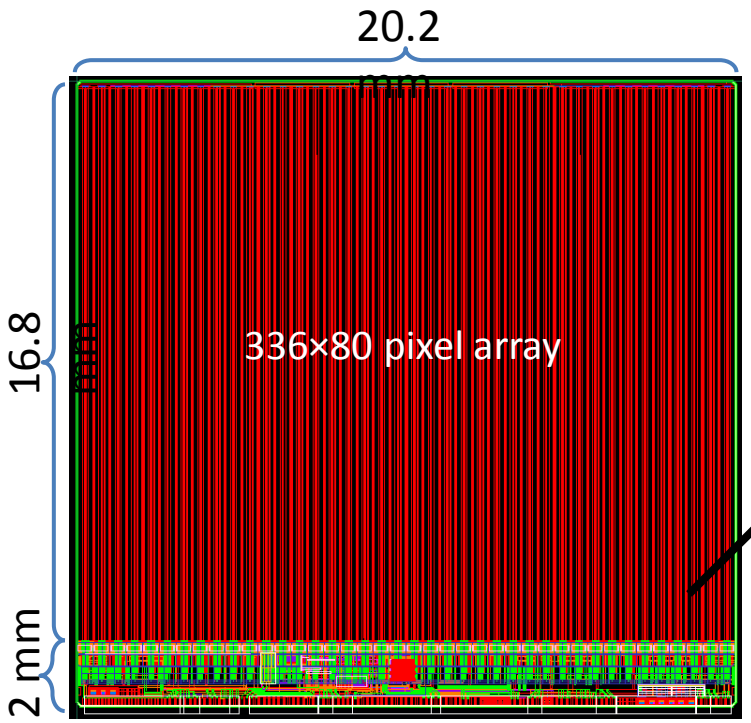
	FE-I3	FE-I4
Pixel Size [µm²]	50×400	50×250
Pixel Array	18×160	80×336
Chip Size [mm²]	7.6×10.8	20.2×19.0
Active Fraction	74 %	89 %
Analog Current [µA/pix]	26	10
Digital Current [µA/pix]	17	10
Analog Voltage [V]	1.6	1.4
Digital Voltage [V]	2	1.2
LVDS out [Mb/s]	40	160

½ current pixel size!

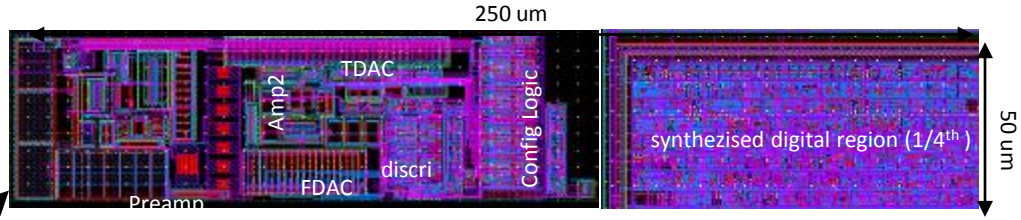
largest in HEP to date

analog / digital power

tuned for IBL occupancy



- Full scale engineering prototype: FE-I4A

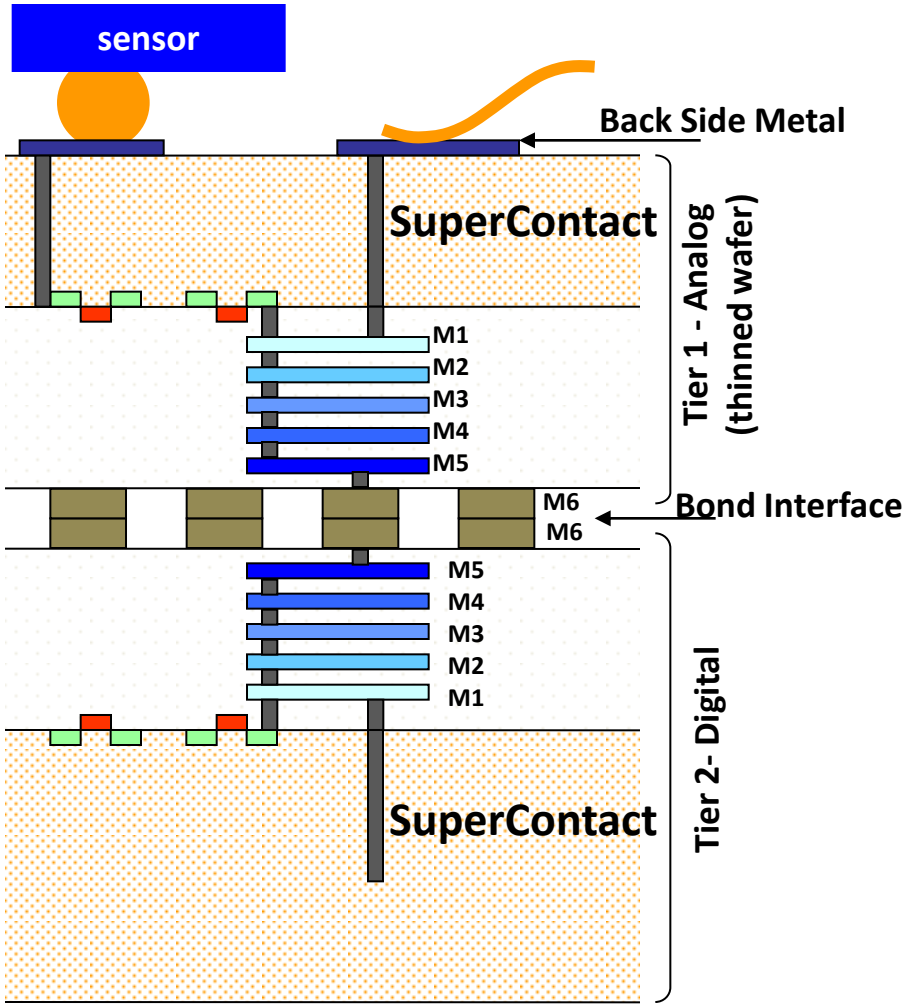


TWEPP 2010 :
Vladimir Zivkovic (NIKHEF)
Laura Gonella (Bonn)
Jens Dopke (Wuppertal)

Karlheinz Meier (U Heidelberg)

ATLAS sLHC Pixel Upgrade : 3D Technology for Smaller Pixels

- Collaboration of Bonn (Germany), CPPM (France) and LBNL (USA).
- Goal: 50×125 µm^2 pixel size with split analog and digital functionalities
- Technology:
  - Chartered 130nm
  - Tezzaron 3D
- Prototype submitted in std. Chartered 130nm technology as a test bench: ➔ Good performance
- 3D analog + digital stack submitted, processing has started

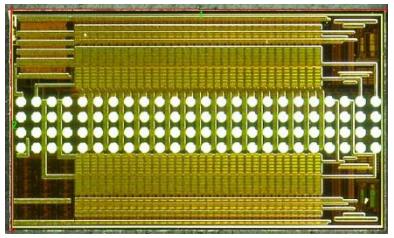


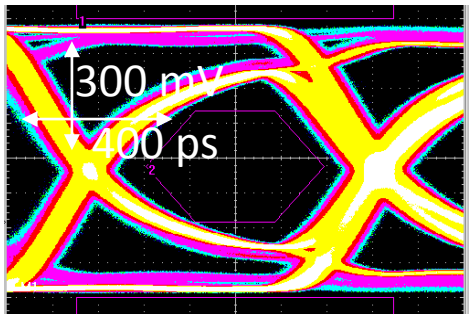
Karlheinz Meier (U Heidelberg)

Karlheinz Meier (U Heidelberg)

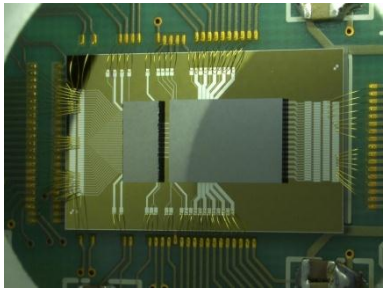
Belle DEPFET Vertex Detector
Complete Electronics Chain (Barcelona, Bonn, Heidelberg)

Data handling processor DHP 0.1 (IBM 90nm)
C4 bump bonds, full data processing, Gbit link,
Analog blocks (U Barcelona)





Switcher : radiation-hard switching of on-detector 20 V signals



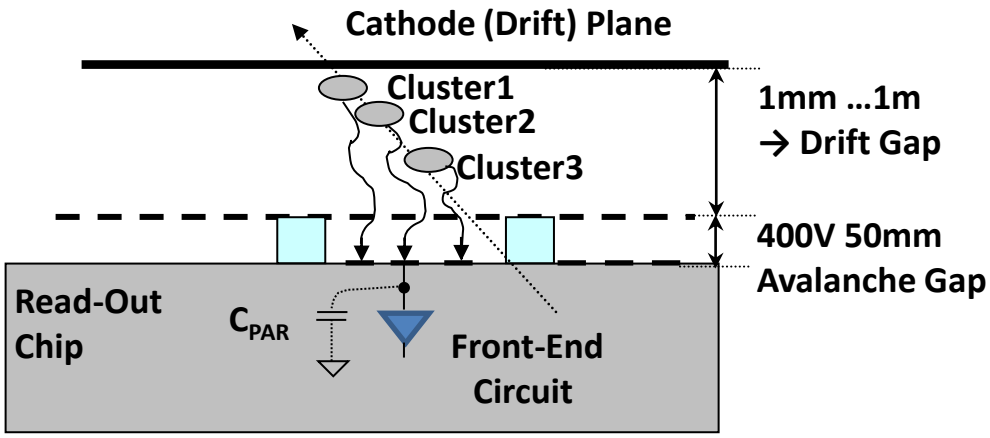
DEPFET Current Digitiser (DCD)
256 channels, 10-bit, 10 MHz ADCs, 65 400 MHz Links

TWEPP 2010 : Jochen Knopf (Heidelberg)

Read-Out of Micro-Pattern Gas Detectors

Gas-avalanche detector with a CMOS readout pixel array (ILC Study)

Bonn, NIKHEF

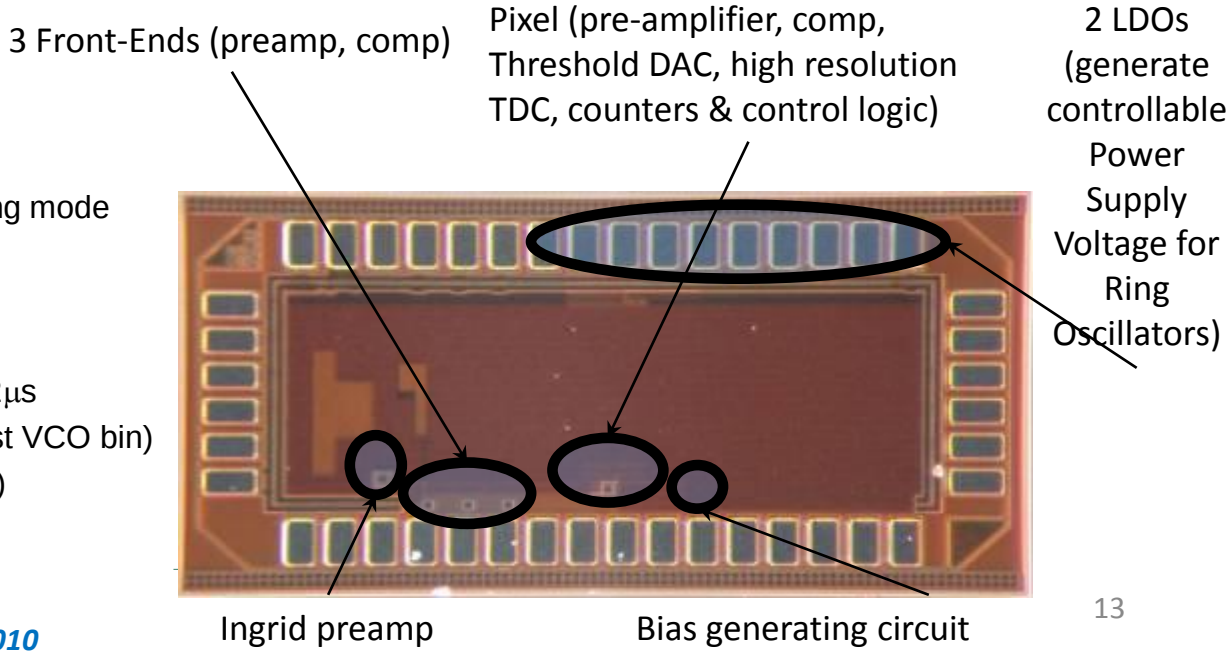


Karlheinz Meier (U Heidelberg)

TWEPP 2010 :
Andre Konrad Kruth (Bonn)

GOSSIPO-3 Test Chip

- Prototype for TPC read-out
- IBM 130nm CMOS (8 metal layers)
- 60μm x 60μm pixels (high granularity)
- Time Measurement mode and Hit Counting mode
- Local TDC in every pixel
- Design Goals:
  - 3μW per channel
  - Arrival time measurement up to 102μs
  - Arrival time accuracy 1.6ns (one fast VCO bin)
  - ToT accuracy 200e^- accuracy (27ns)
- Design effort lead by NIKHEF
  with contributions from Bonn

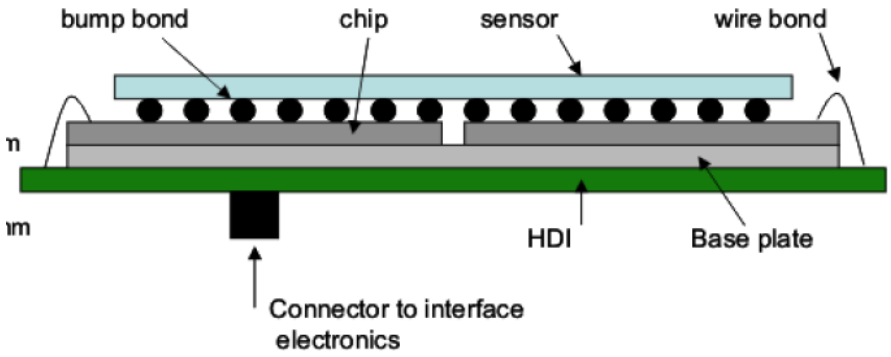


AGIPD (Adaptive Gain Integrating Pixel Detector) for XFEL (DESY)

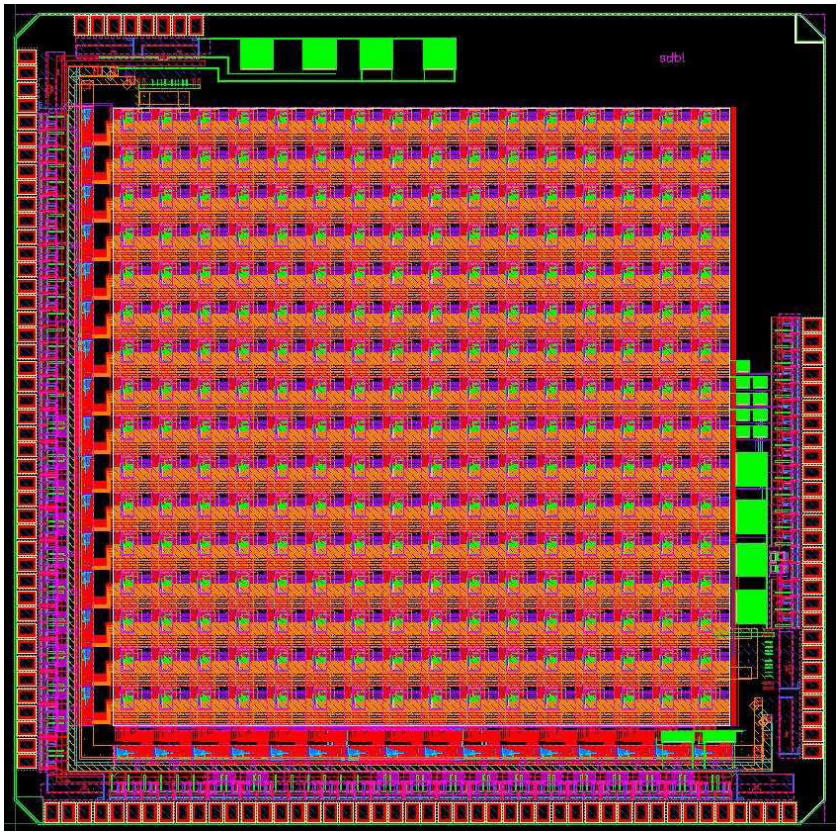
DESY Hamburg und Bonn University

Challenges

- high dynamic range (1 - 1.4 x 10^4)
- single photon sensitivity,
- long storage chain (≥ 200)
- long hold time (99 ms)
- high radiation dose (up to 100 MGy)



Prototype test chip with a 16 x 16 pixel matrix
130nm (IBM cmrf8sf DM) CMOS technology
10 x 10 storage cells / pixel.

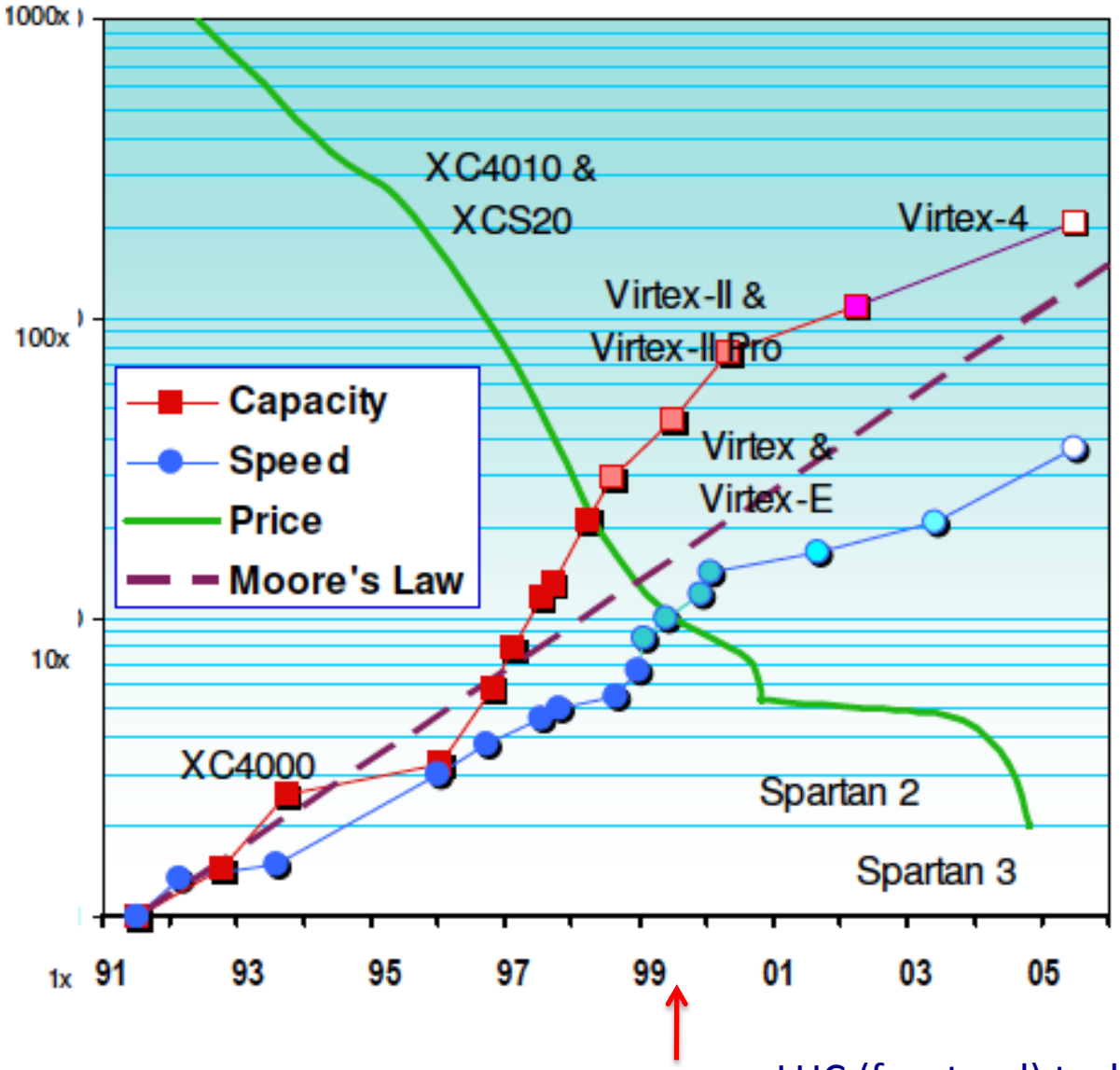


Karlheinz Meier (U Heidelberg)

TWEPP 2010 : Peter Goettlicher (DESY)

FPGAs

Rise of FPGAs



The Rise of Field Programmable Gate Arrays

Logic x 200

Speed x 40

Lower Power x 50

Lower Cost x 500

S. Trimberger (XILINX)

many LHC (frontend) technology decisions

ATLAS – Level-1 Calorimeter Trigger Upgrade (Heidelberg)

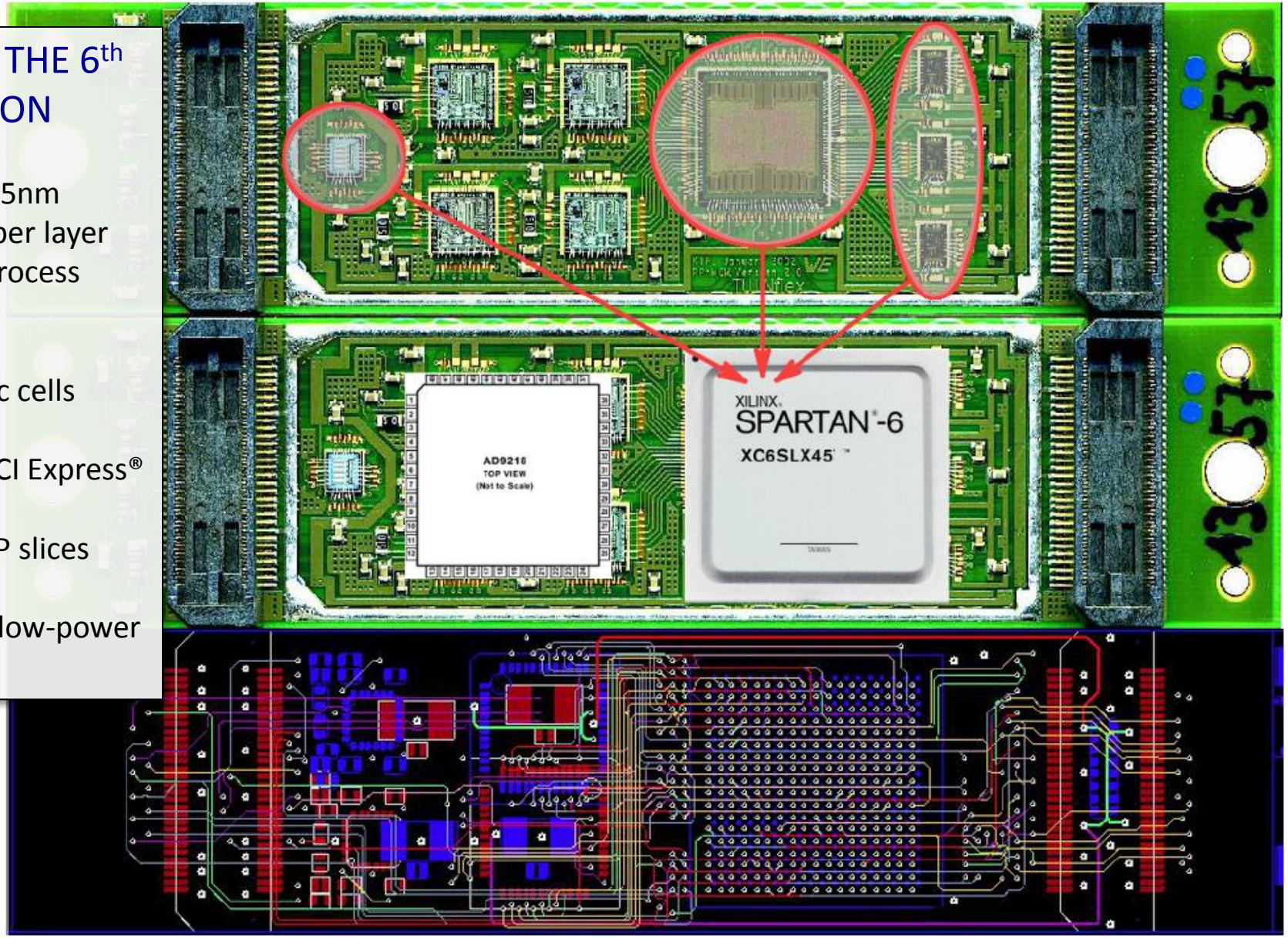
SPARTAN- THE 6th GENERATION

low-power 45nm
9-metal copper layer
dual-oxide process technology

150,000 logic cells

integrated PCI Express® blocks
250 MHz DSP slices

3.125 Gbps low-power transceivers



Silicon Photo-Multipliers
Avalanche Photo-diodes

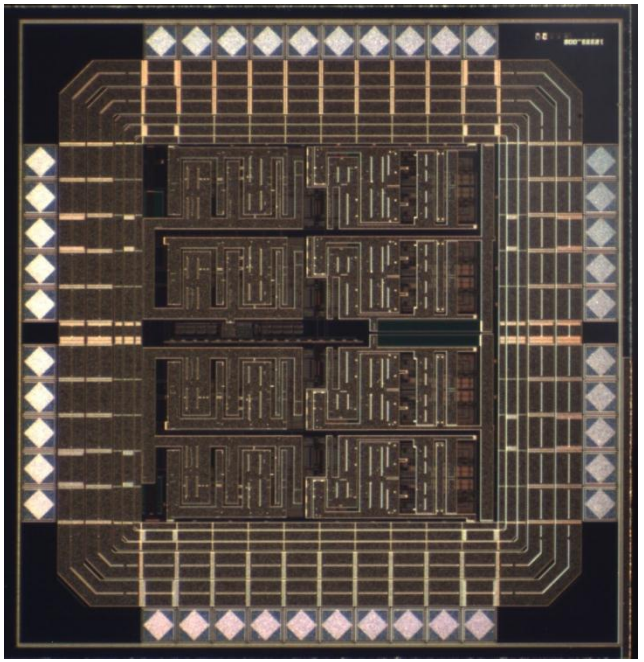
Silicon Photomultiplier Readout Systems U Heidelberg

CALICE

KLauS: Charge Readout Chip
[Kanäle für Ladungsauslese von SiPMs]

AMS 350nm CMOS technology; 4 channels;
SPI interface controlled by FPGA; Bias DAC tunable;
high Signal/Noise Ratio [>10, 40 fC signal charge];
fast trigger available [pixel signal jitter < 1ns];
large dynamic range up to 150pC

Upgrade version to be part of SPIROC III
S. Callier et. al, IEEE NSS/MIC, 2009;
0.1109/NSSMIC.2009.5401891

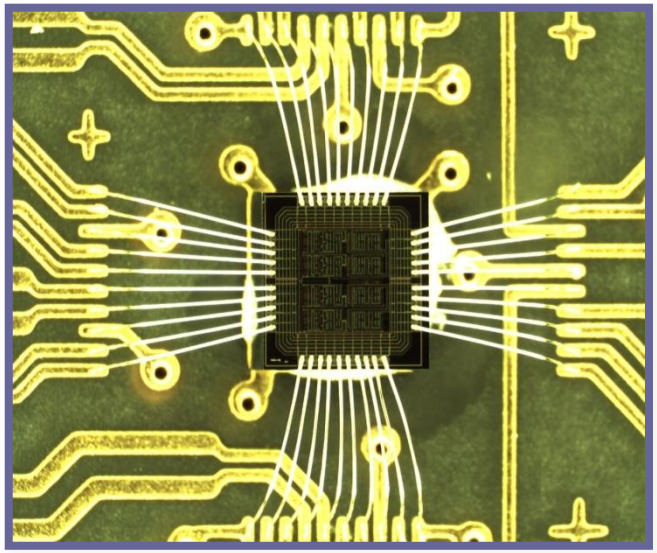


PET and ToF

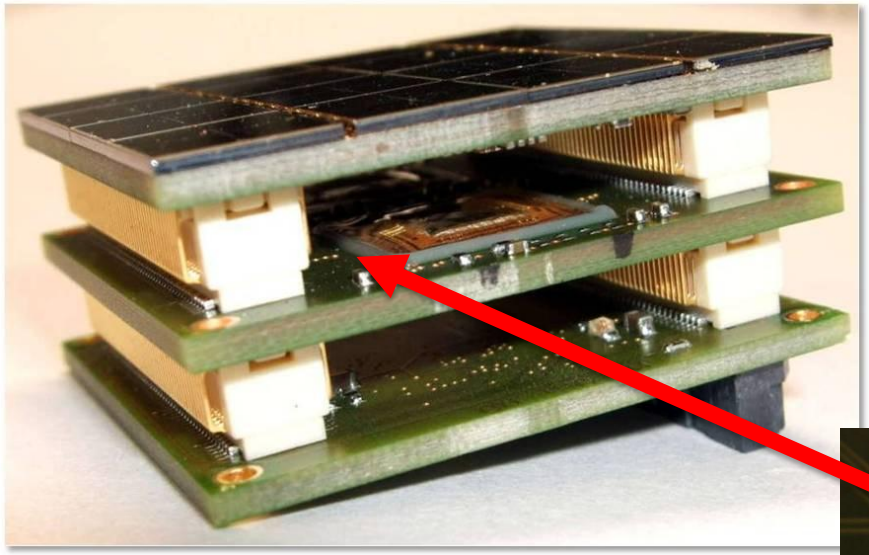
STiC: SiPM Timing Chip
[Fast Discrimination for ToF]

AMS 350nm CMOS , 4 channels;
Leading edge & Constant fraction Trigger;
Bias DAC tunable ~ 1 V; power < 10mW/ch
Pixel jitter ~300 ps, time of flight capability

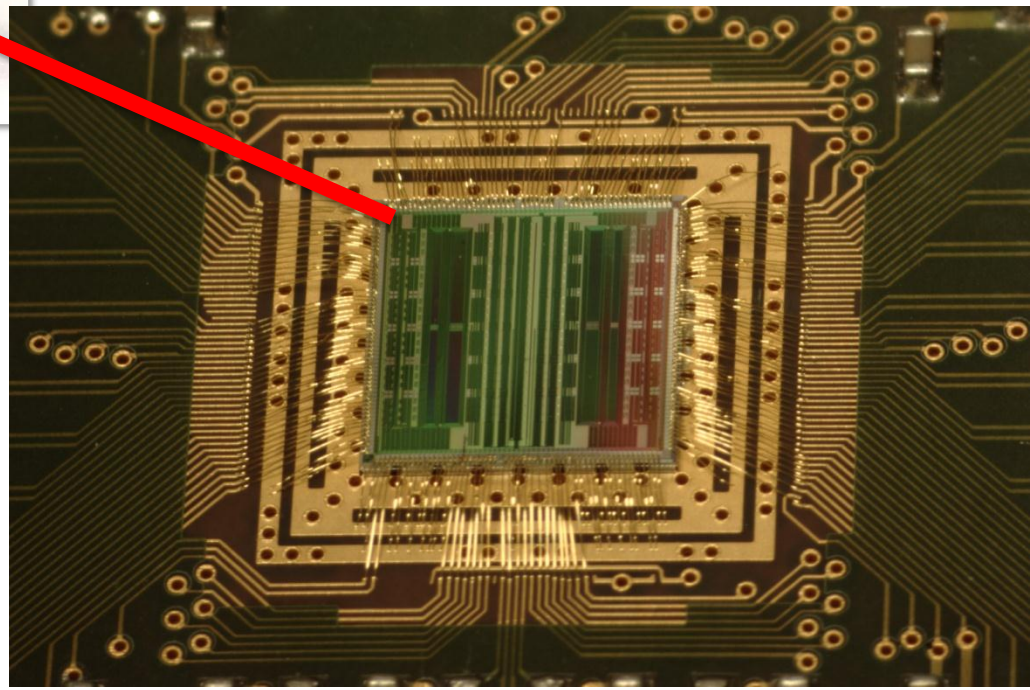
W. Shen et. al, IEEE NSS/MIC,
2009; 10.1109/NSSMIC.2009.5401693



Readout of APD Array for PET-MR (U Heidelberg)



Karlheinz Meier (U Heidelberg)



40 Channel Readout Chip

- fast low-noise differential amplifiers
- O(100µV noise)
- time stamping with 50ps binwidth
- integrator
- > 9Bit ADC

HEP in Germany

Particle Physics in Germany

Grav. Waves

HESS, MAGIC

Bottom, Charm, Kaon

Nuclear Structure

Auger, Icecube ..

HERA, Tevatron,

CRESST,

LHC, ILC

Heavy Ions, Antiprotons

ν Oscillation, mass

Compass,Her mes, Hadrons

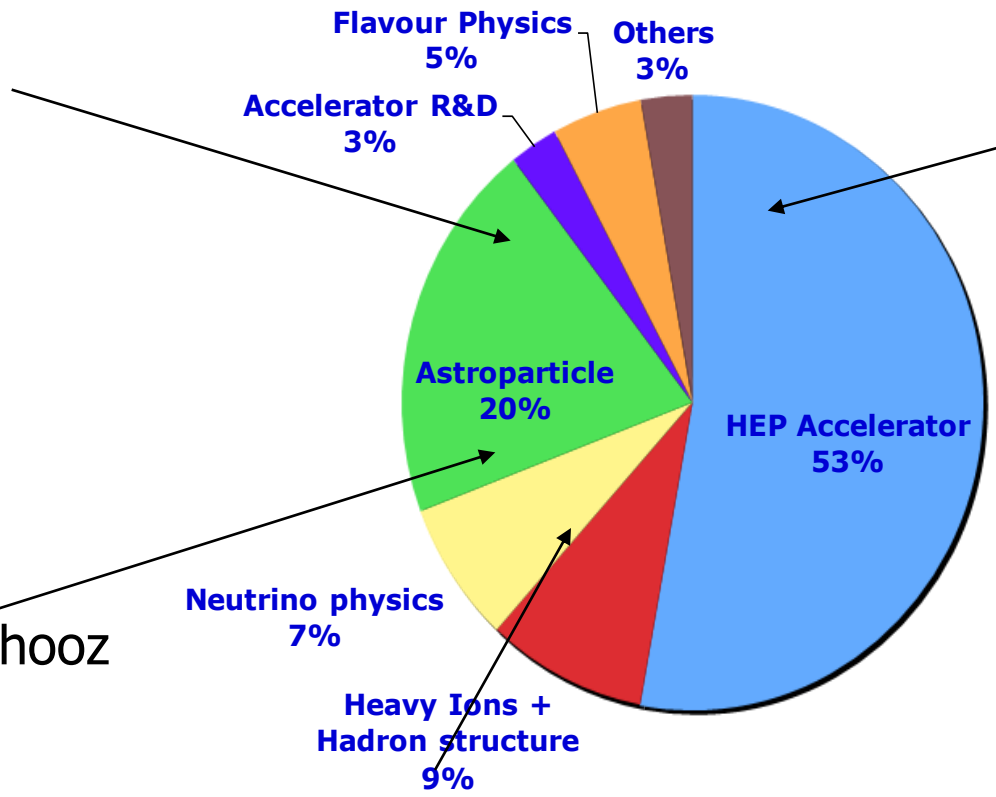
+ R&D on Accelerator, detector, (Grid) computing

Bernhard Spaan (TU Dortmund)

See also P. Mättig 2006 RECFA review

Fields of Research (HEP)

2006



HESS
MAGIC
Auger
IceCube
CTA
…

Mainly LHC
ATLAS, CMS,
LHCb
- upgrades

HERA,
Tevatron
B-Factories
(BABAR + BelleII)
ILC
…..

Double Chooz
OPERA
KATRIN
…

Incl. ALICE

Bernhard Spaan (TU Dortmund)

DESY

Changing role of DESY

Now: no operating accelerator for particle physics
accelerators at DESY $\rightarrow$ photon science

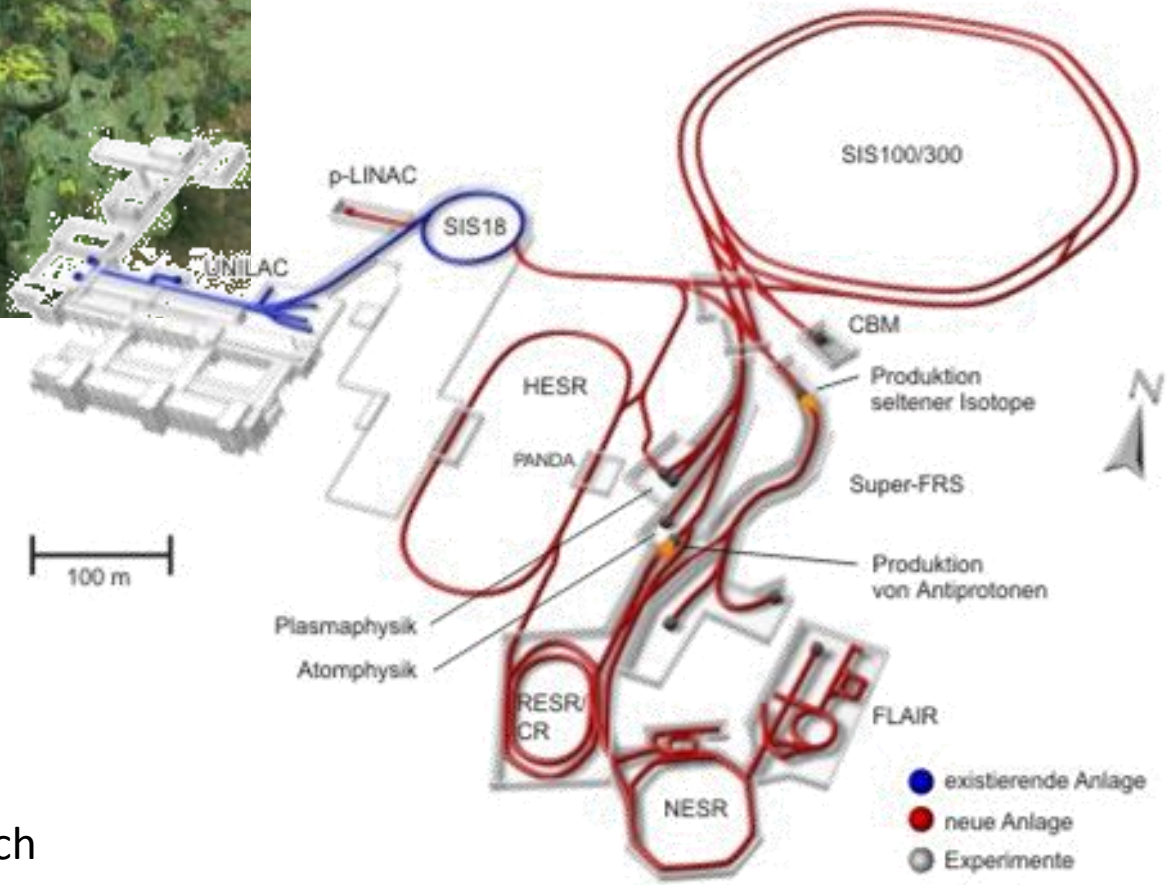
HERA data still being analyzed

Still vital for particle physics in Germany
- central facilities
  - (e.g. Tier-2 Center for ATLAS, CMS, LHCb)
- National Analysis Facility
- Heart of the Helmholtz-Alliance

Bernhard Spaan (TU Dortmund*)*

Foundation: 4.10.2010

Mostly not particle physics
Complex detectors required though



GSI & FAIR

FAIR

Facility for Antiproton and Ion Research

Conclusions

Strong research in particle physics

Strong focus on LHC programme (incl. Upgrade)

DESY changed profile – still vital for particle physics
Free Electron Laser development (ndr)

Somewhat complicated structure/funding regime

Participation in all areas –

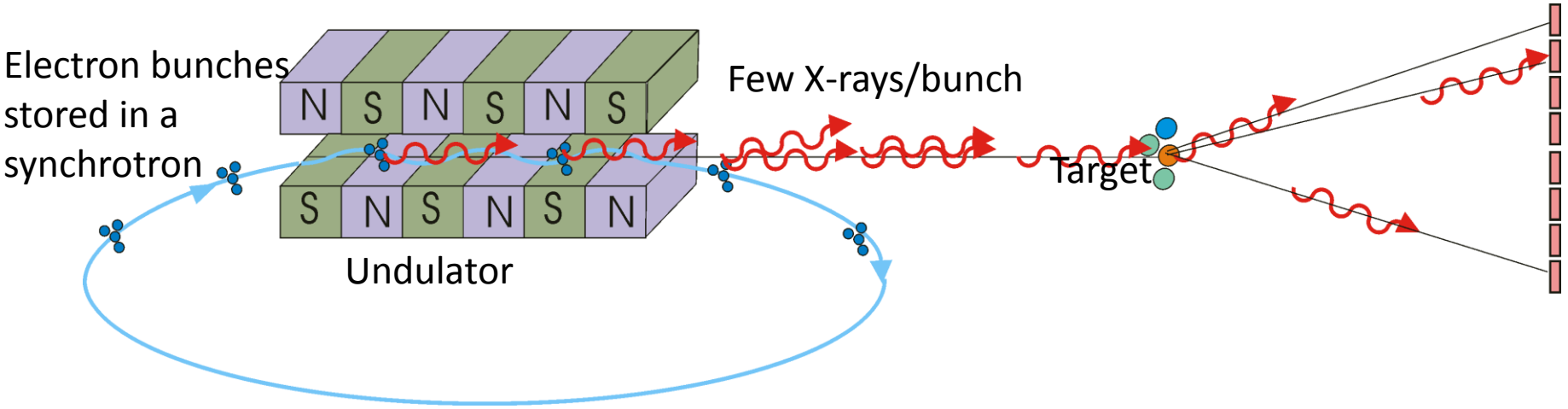
- Detector R&D and construction
- Electronics
- Data Analysis
- Computing
- Accelerator Physics

Bernhard Spaan (TU Dortmund*)*

Future strategy in preparation

The Free Electron Laser (FEL)

Science with X-ray from nowadays synchrotrons 3rd Generation



- **Nice systems,**
  but more wishes for the future
  - Intensity
  - Coherence for holography
  - Many photons/bunch in <100fs:
    ⇒ Get the picture before X-rays destroy the target

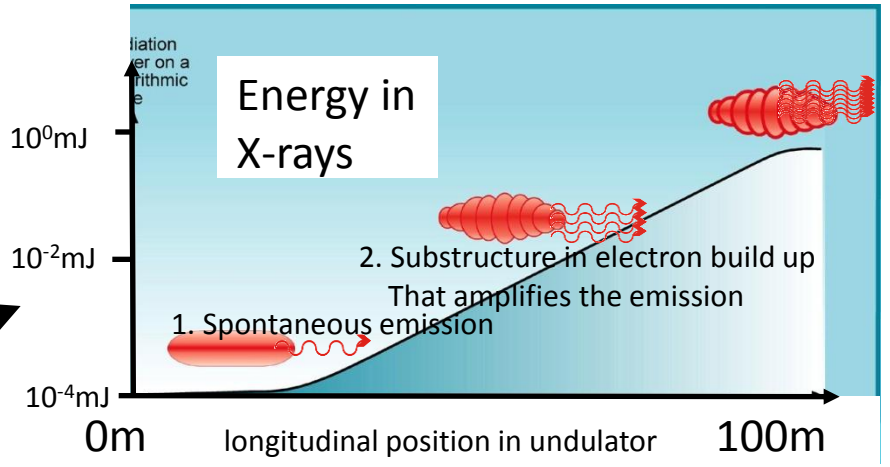
Imaging detectors:
e.g. Pilatus:
2-dimensional pixel
Counting: 1MHz/pixel
Rate: 10-100 pictures/sec

The Free Electron Laser

The SASE principle

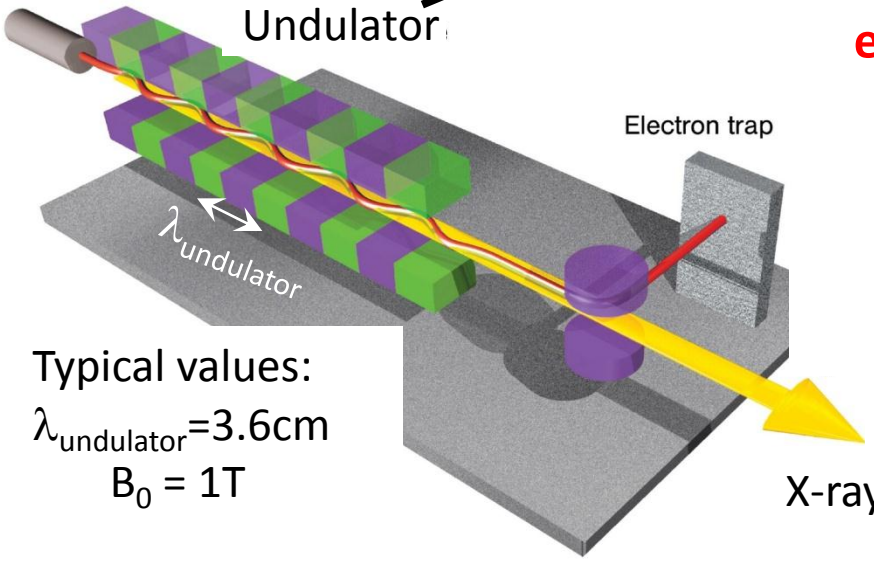
Self amplified spontaneous saturation emission

Lasing for X-ray FEL's needs very dense electron bunches at moderate energies



Electron source + accelerator

Undulator



Typical values:

$\lambda_{undulator}$=3.6cm

B_0 = 1T

Basic requirements, for electron source and accelerator

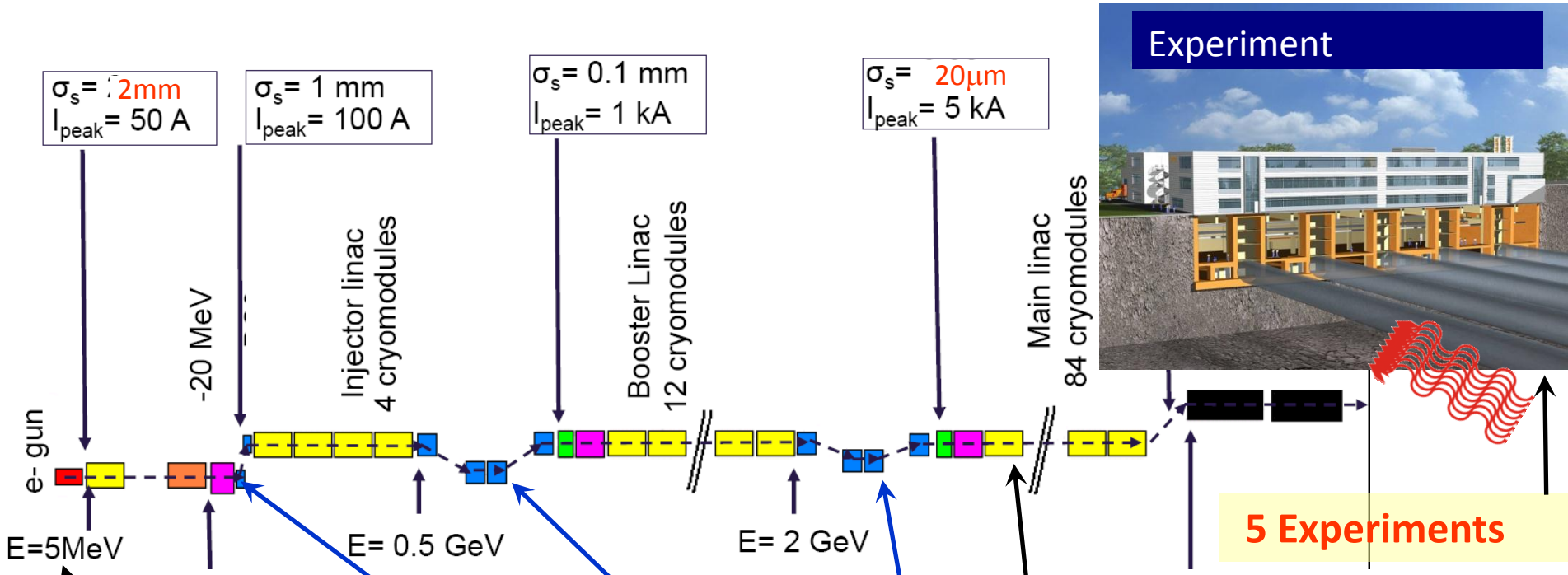
$$\lambda_{X-ray} = \frac{\lambda_{undulator}}{2\left(\frac{Ee}{m_e c^2}\right)^2}\left(1+\frac{K^2}{2}\right) \quad with \quad K = \frac{eB_0\lambda_{undulator}}{2\pi\, m_e c} = 1...10$$

- Wavelength 0.1nm: **17.5GeV** electrons

- Power grows with current density $\propto e^{\sqrt[3]{j}}$ ..... Short bunches ~20µm with Q=1nC

  20µm converts to 70fsec

XFEL: Functional blocks



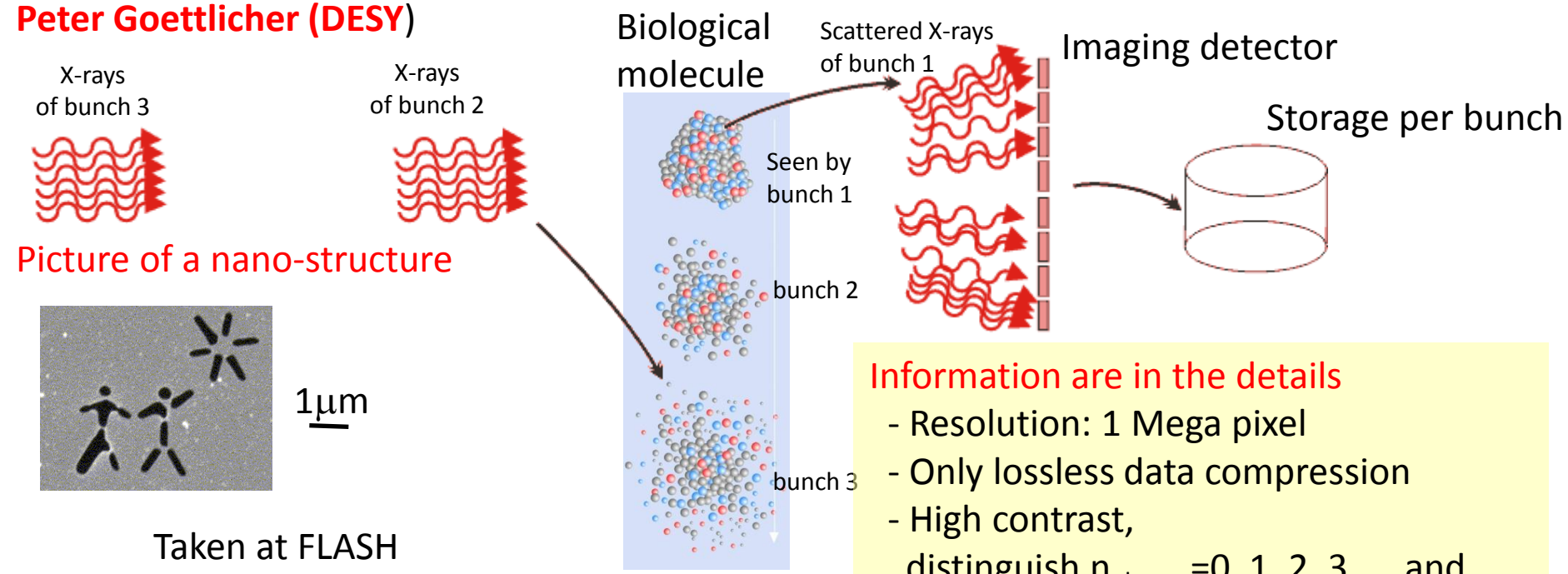
Electron-source:
- Laser to a photo cathode
- Immediate acceleration

Bunch compression
- Position to energy
- Different path-length through magnetic chicanes

Acceleration
By superconductive RF-cavities: 1.3GHz

Detectors for the dream: 2-dimensional cameras

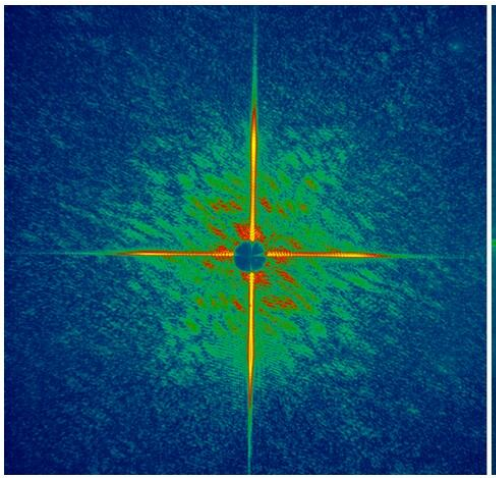
Peter Goettlicher (DESY)



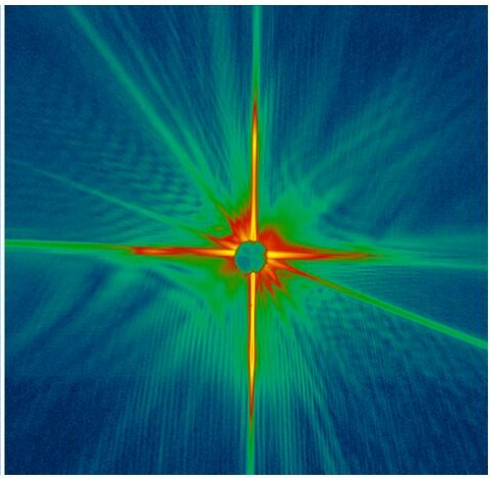
Picture of a nano-structure

Taken at FLASH

First hit



Melted foil



Information are in the details

- Resolution: 1 Mega pixel
- Only lossless data compression
- High contrast,
  distinguish n_{photon}=0, 1, 2, 3,…. and
  for high signals statistical limit

$$resolution < \sqrt{n_{photon}}$$

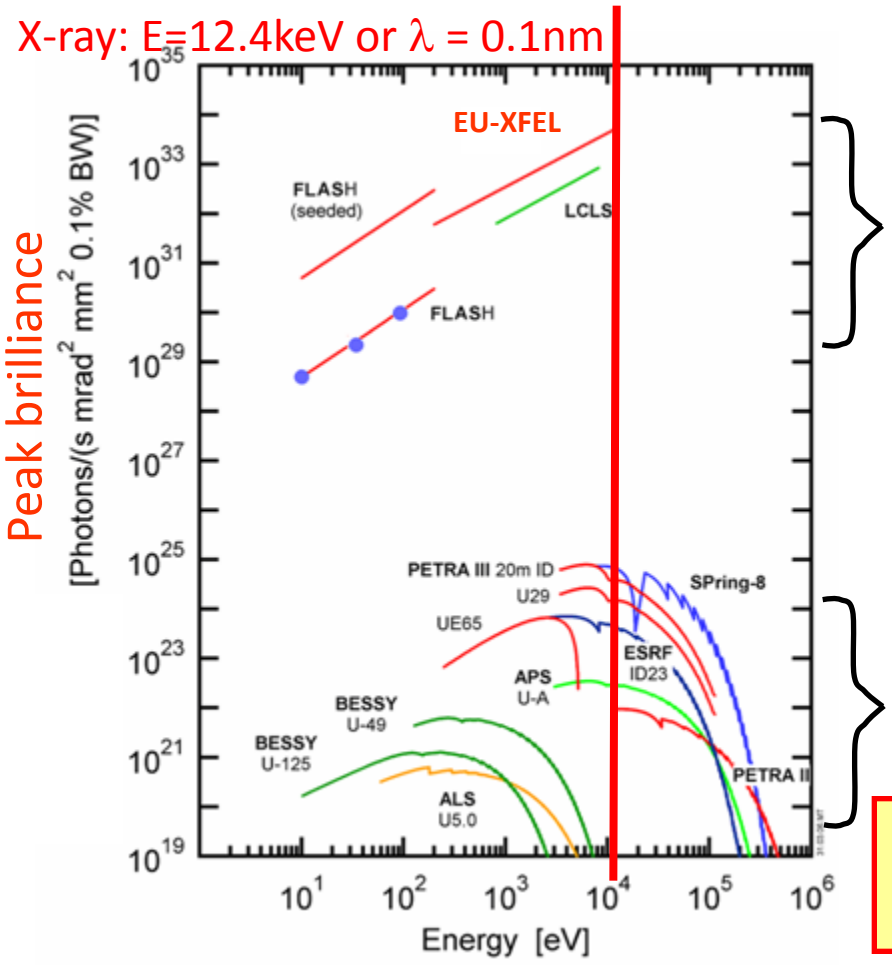
- Many pictures, but objects differ
  e.g. in position/orientation x,y,z,θ,φ
- Complex analysis before combining,
  only offline?

Consequences:

- **Need to store every 220ns a picture**
- **Select the best ones to reduce to reasonable data volume 80Gbit/s**

Comparison: From synchrotrons to FEL's

Intense light gets delivered by lasers,
now lasing for X-ray



FEL based sources

LCLS: Operation since 2009: X-ray
SLAC, USA

SCSS: Planned for 2011, X-ray
Spring-8, Japan

FLASH: Operation since 2005: VUV-light
DESY, Germany
User-operation and
test facility for XFEL

European XFEL

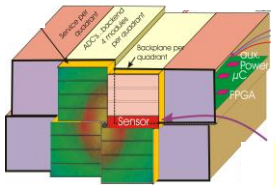
Construction until 2014/15: X-ray
DESY, Germany

Synchrotron based sources

9 orders of magnitudes
Good reason to build new accelerators

The European XFEL:

General detector concepts: Electrical and Connectivity

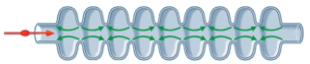


Bump bond/pixel

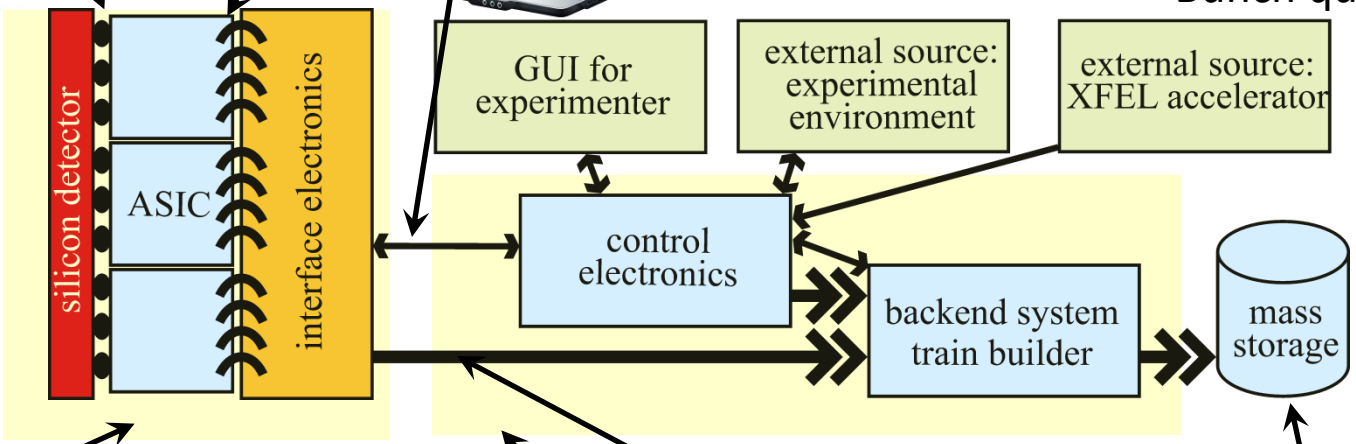
Copper cables
Clocks, TCP/IP-100MbE

Wire bonds to a
High-Density board

Environment
Scattering quality



Sync. clocks
Bunch quality



Camera head
- Three consortia for cameras
- Each covering multipurpose science, each not all, all differently specialized

Fibre optics
UDP-10GbE

Crates in racks

Common development
for all at XFEL-experiments

IT-center

2-dimension cameras

AGIPD

Adaptive Gain Integrated Pixel Detector

Institutes: Bonn(University), DESY, Hamburg(University), PSI(Villingen)

Reference: B. Henrich, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.06.107

DSSC

DEPMOS Sensor with Signal Compression

Institutes: MPI-HLL Munich, DESY, Heidelberg(Univ.), Poly. Milano, Bergamo(Univ.), Siegen(Univ)

Reference: M. Porro, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.02.254

LPD

Large Pixel Detector

Institutes: STFC/RAL, Glasgow(University)

Reference: S.R.Burge et al., Large Pixel Detector for the European X-ray Free Electron Laser, 11th European Symposium on Semiconductor Detectors, June 2009 conference proceedings.

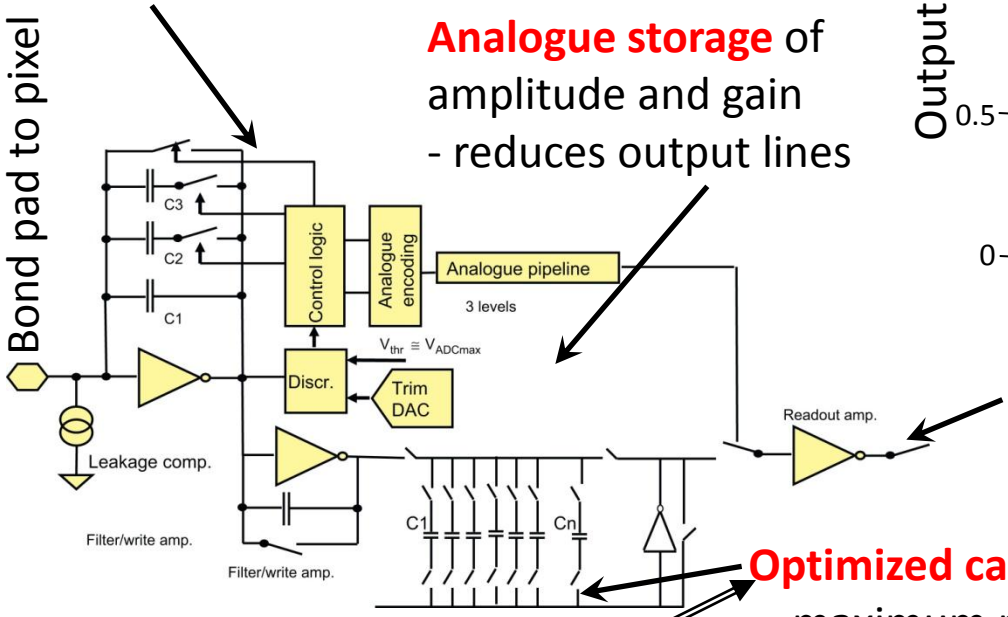
Common items: Sensor-studies, **ASIC in 130nm-technology**, DAQ-systems

Different physics by different technical approaches

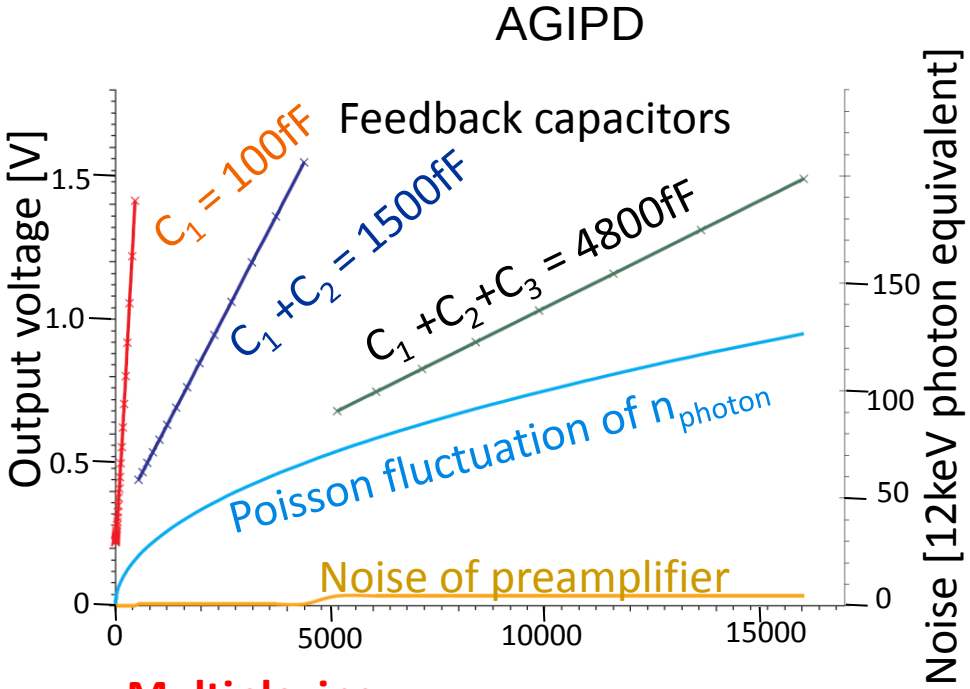
	AGIPD	DSSC	LPD
Pixel	200 x 200μm^2	236μm hexagons with a DEPFET	500 x 500μm^2
Approach for dynamic range	Automatic gain switching	Compression by DEPFET in pixel	3 parallel gains
Storage per bunch	Analogue with analog ASIC-out.	Digital, 1ADC/pixel	Analogue with digital ASIC-out.

Camera Analog ASIC

Automatic gain switching:
- Gain switches,
  when output exceeds threshold
- Adding instead of replacing capacitors
  avoids charge losses



Analogue storage of amplitude and gain
- reduces output lines



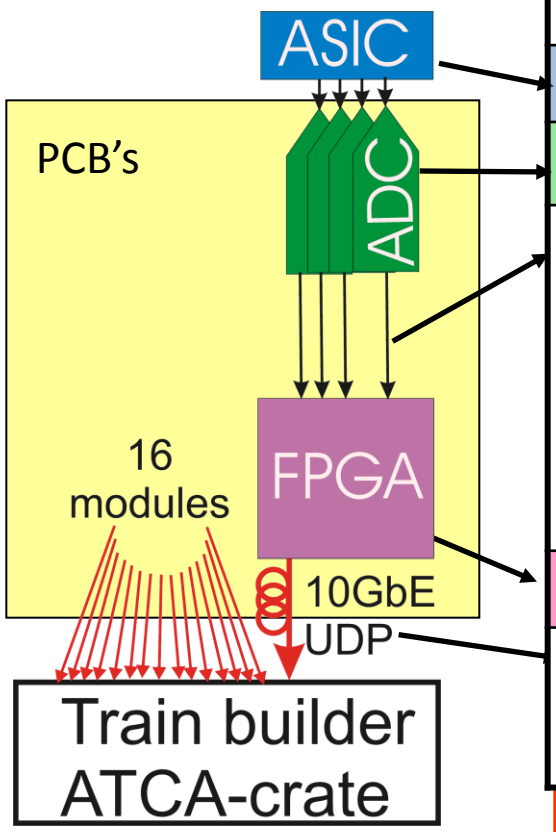
Multiplexing:
Just one differential output
For 32 x 32 pixels

Optimized capacitors to store
maximum number of picture of a train
not all 2700 will be possible
realistic: ~ 200

Constraint
Everything has to fit behind
the pixel 200µm x 200µm

Random address overwriting allows handling of an external decision of best scatterings

Signal rates



Devices or links in		Rates per		
module	Detector head	link	module	Detector head
16	256			
64	1024	0.05	3.2	**51.2 GS/s**
64	1024	0.7	45	**720 Gbit/s** While digitizing (10% duty cycle) Data written to RAM by
1	16			
1	16	5	5	**80 Gbit/s** Continuously

Very high internal data rates require plenty parallel lines

Still high continuous data flow to crates:

requires modern data transfers: 10Gbit/s on fibres

and high performace crate electronics: xTCA

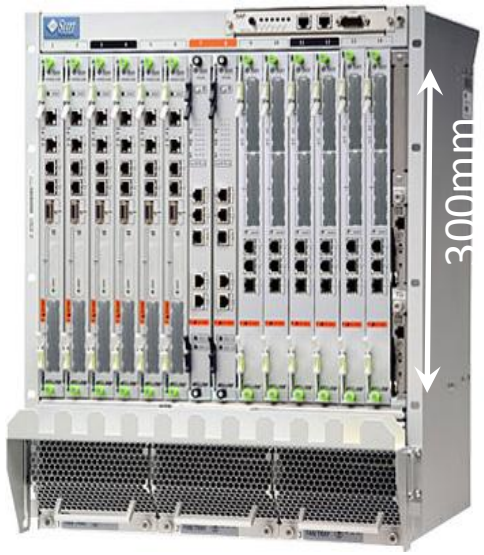
xTCA as platform

High performance digital standard: Telecommunications

- ATCA: **A**dvance **T**elecommunication **C**omputing **A**rchitecture: 2002

Features:

- Backplane: many multi gigabit serial links
- Configurable network
- Redundancies: Power, CPU, MCH
  Reliability >99.999%
- Carriers for 1-8 AMC
  Advance Mezzanine Cards
- Hot swap



µTCA

Scalable to

- Small systems
- Features like ATCA
- modules = AMC's

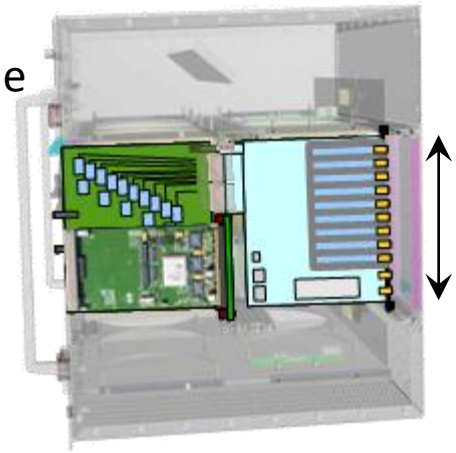
A standard for physics

- Science (European XFEL) + Industry)

Features:

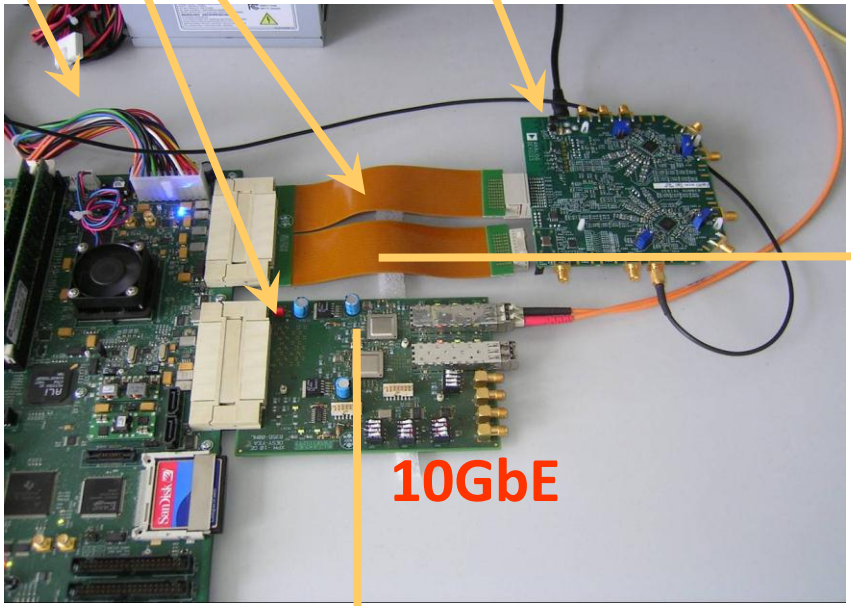
- Based on µTCA
- More space
- Synch. clocks on backplane
- Rear access by µRTM's
  µRear Transition Modules

Double size AMC

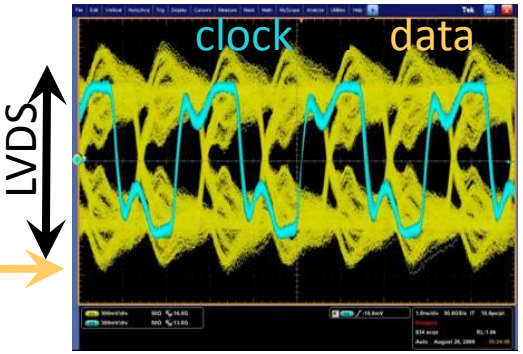


Evaluation of high speed data transfers

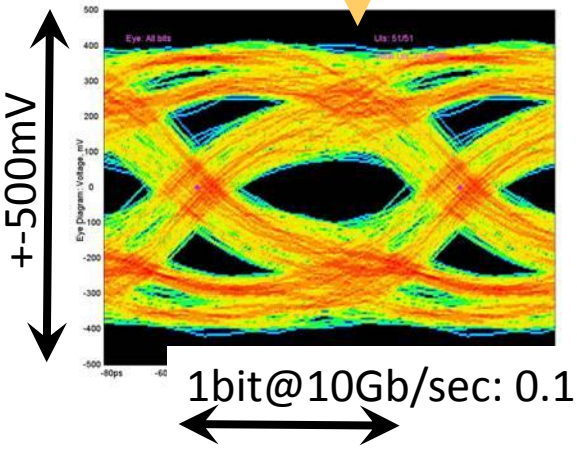
XILINX evaluation board + custom VHDL-UDP-core
+custom designs+ ADC-evaluation board



ADC: 700Mbit/s



Performance limited by no-impedance on XILINX-evaluation board
Eye diagram is well open



10 Gbit-Ethernet

… Measurement is limited by 16GHz-scope
Performance is better
Eye diagram is well open

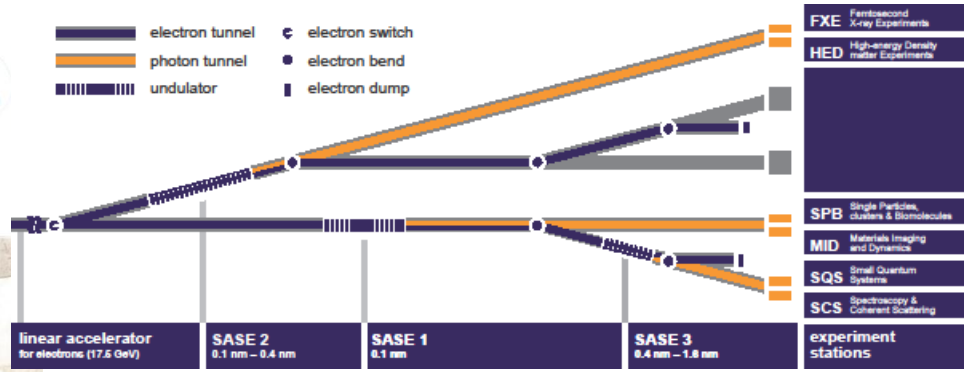
Links are OK.

- Need no ideal setup
- Freedom to optimize system setup mechanics, modularity,…

XFEL status

- European XFEL will deliver the highest peak brilliance and bunch rate.
- Need of excellent accelerator performance: Size and energy of bunch.
- Dedicated regulations in modern technologies needed.
  Developments and tests at FLASH are on going with good results.
- That leads to the use of modern standards in science: ATCA, μTCA.
  Adapting them to the needs (PICMG®) and first modules are available.
- Demanding dedicated detectors (Pixel cameras) are being developed.
  Ongoing developments for full chain with high signal and data throughput:
  - Sensors, ASIC's, detector heads and DAQ systems
  - e.g. 4.5MHz picture rate, 80 Gbit/s out of small detector heads
- All the effort opens new fields of science:
  Capturing a scattering picture with one flash of X-rays.
- Thanks to all the work packages and consortia for providing material
- More information on www.xfel.eu
  http://hasylab.desy.de/instrumentation/detectors/index_eng.html

XFEL plans



Many more to be done,

by two drilling machines

2012 Buildings getting ready for installation

2013 First beam in injector

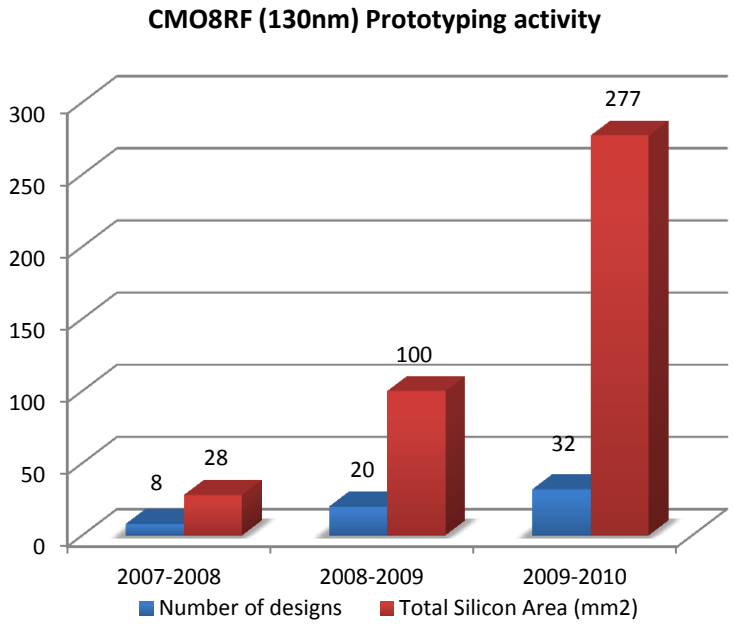
2014 First beam in linear accelerator

2015 First SASE, first experiment

2016 'Full' User operation

Multi-projects, ASICS, 3D

CERN Microelectronics Users Group



- **IBM 130nm design kit version 1.7**

- **Scripts for mixed design available**

- **Develop a scripted design for digital core circuits with separate substrate ground for low noise applications.**

- **Develop an IP library in IBM 130nm CMOS**

Forthcoming MPW runs:

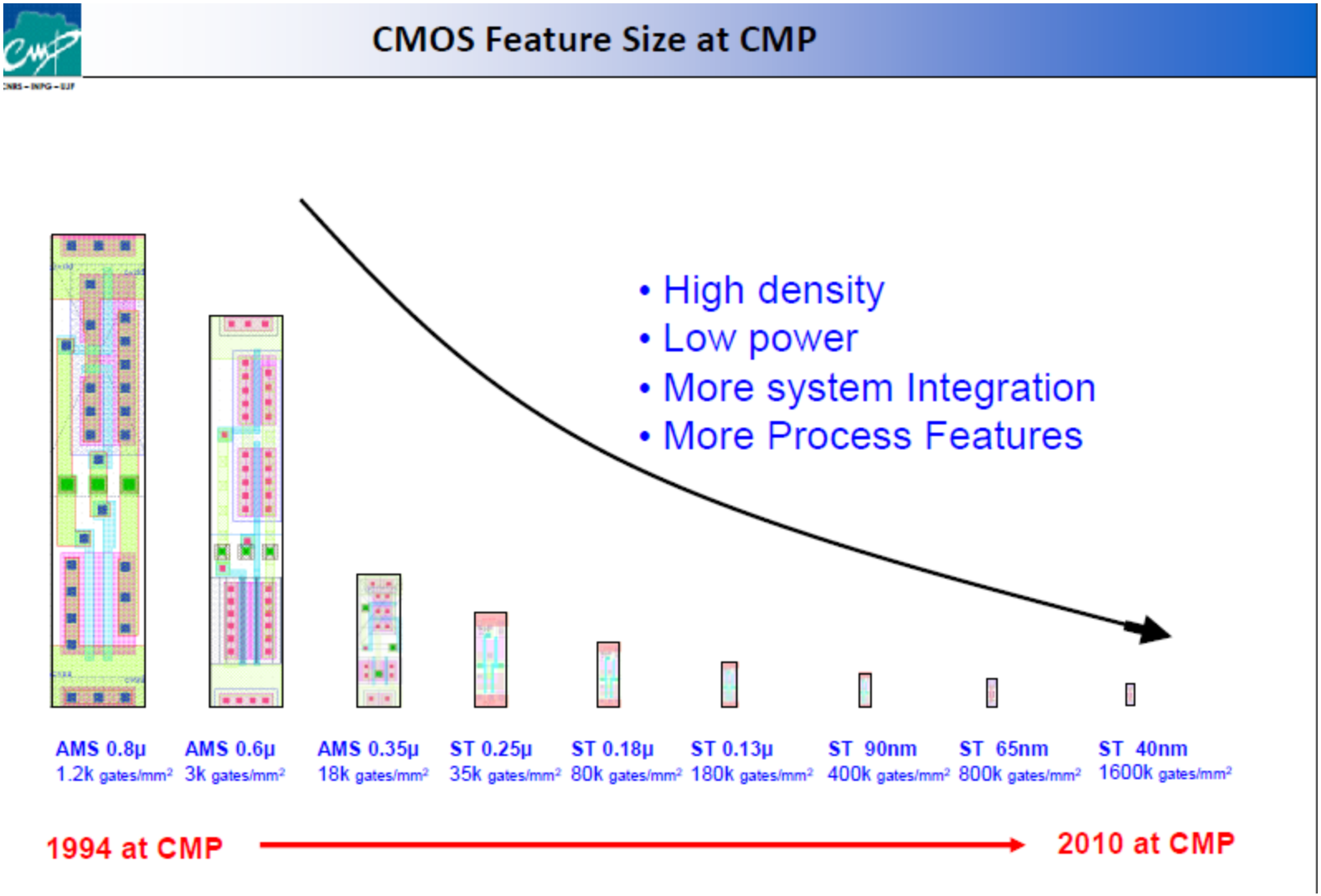
CMOS6 (250nm)
Tape Out beginning of next year.
Support for 3 and/or 6 metal stacks.
CMOS8RF (130nm)
MOSIS Nov. 8, 2010
CMOS9LP/RF (90nm)
MOSIS Dec. 8, 2010

Forthcoming AMS Workshops

Week of Oct. 18-22
End of 2010

Kostas Kloukinas (CERN)

CMOS feature size evolution 1994-2010



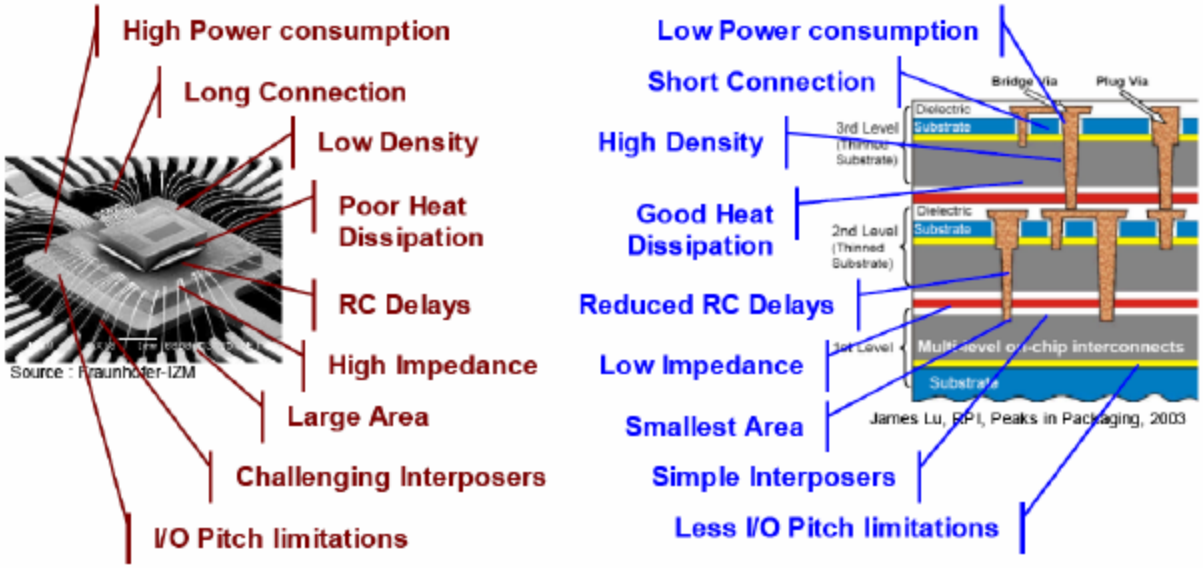
Kholdoun Torki (CMP Grenoble)

Conventional interconnections versus 3D

SiP versus 3D-IC

Why TSV Interconnection?

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

Page3

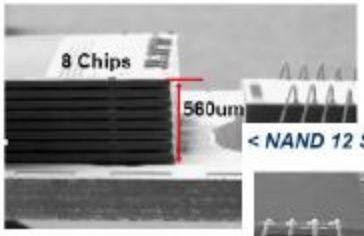
Kholdoun Torki (CMP Grenoble)

3-D MPW Industrial Applications

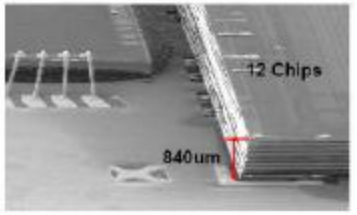
Industrial Applications

- There are two 3D areas that are receiving a lot of attention.
  - Stacked memory chips and memory on CPU
    - IBM expected to provide samples later this year
    - Both IBM and Samsung could be in production next year (2008)
  - Imaging arrays (pixelated devices)
    - Working devices have been demonstrated by MIT LL, RTI, and Ziptronix
    - Much work is supported by DARPA
- Pixel arrays offer the most promise for HEP projects.

< NAND 8 Stacked Memory Card >

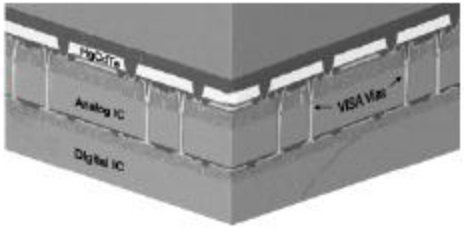


< NAND 12 Stacked Memory Card >



Samsung - 30 um laser drilled vias in 70um chips

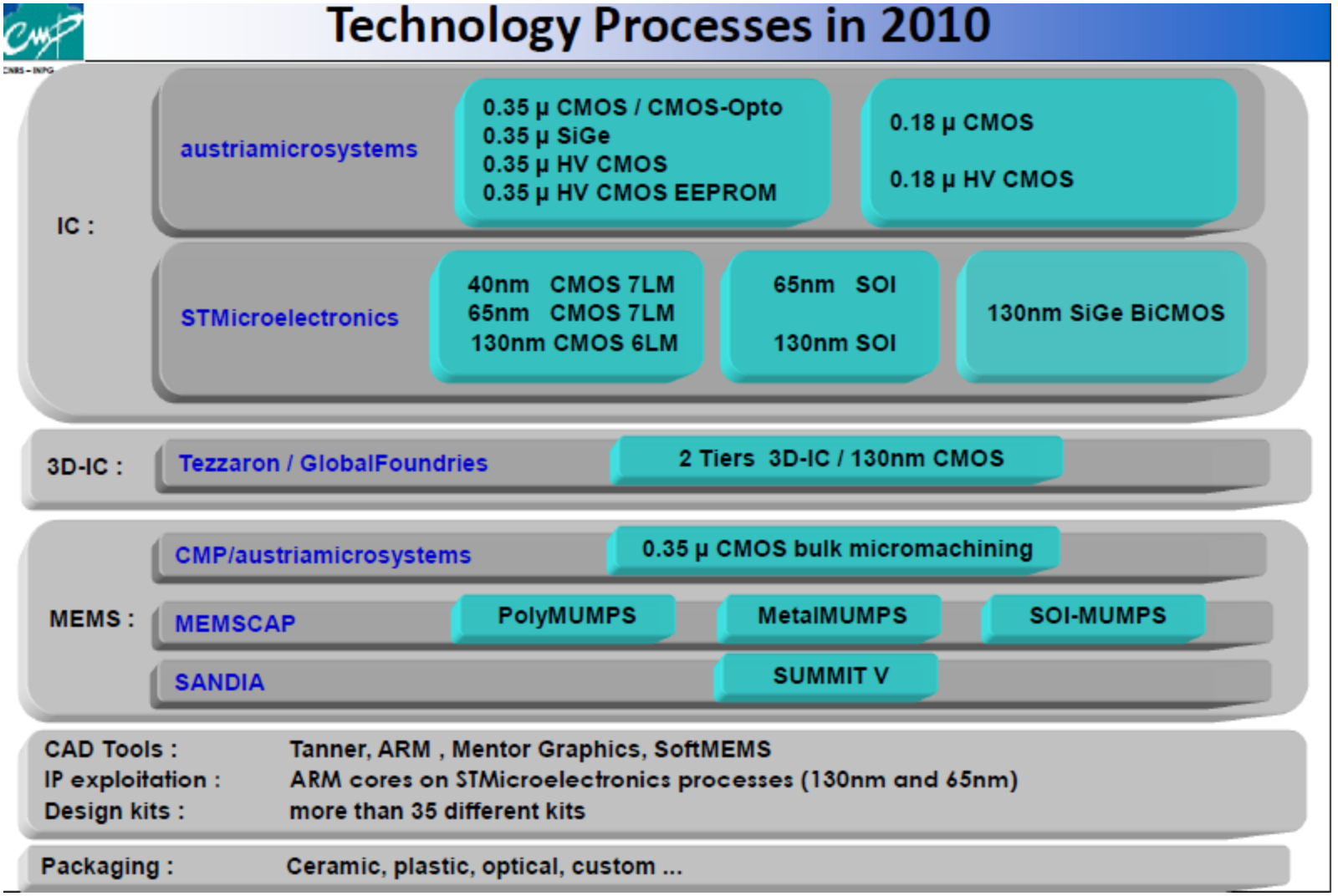
RTI Infrared Imager



LHC-ILC Workshop on 3D Integration Techniques

Kholdoun Torki (CMP Grenoble)

3-D Multi-Project Wafers runs for HEP



Kholdoun Torki (CMP Grenoble)

3-DMPW Access

CMC-CMP-MOSIS partnering on 3D-IC

CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

The first MPW run is targeting January 2011:

- 2-tier face-to-face bonded wafers
- 130nm CMOS process for both tiers
- Top tier exposing TSV and backside metal pads for wire bonding.

A design-kit supporting 3D-IC design with standard-cells and IO libraries is available.

Further MPW runs will be scheduled supporting process flavors (multiple tiers beyond 2, different CMOS flavors for different tiers, ...) driven by user requirements.

Potential users are encouraged to contact **CMP** for details : **cmp@imag.fr**

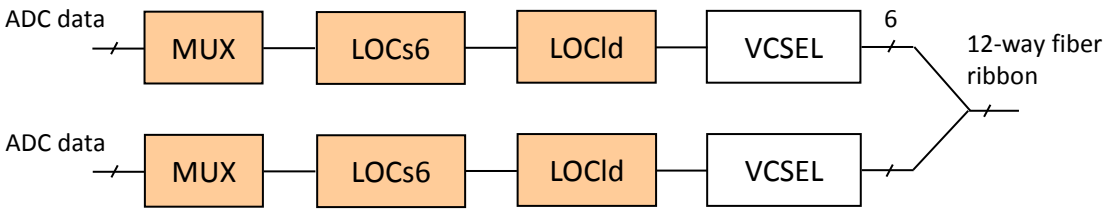
Kholdoun Torki (CMP Grenoble)

Fast optical serial links

LOC6 project

Proposed for the upgrade ATLAS/LAr FEB optical link: 100 Gbps/FEB bandwidth = 62× LHC

- ASIC technology as 0.25 µm silicon-on-sapphire CMOS technology commercially available, MWP runs ~ 6 /year.



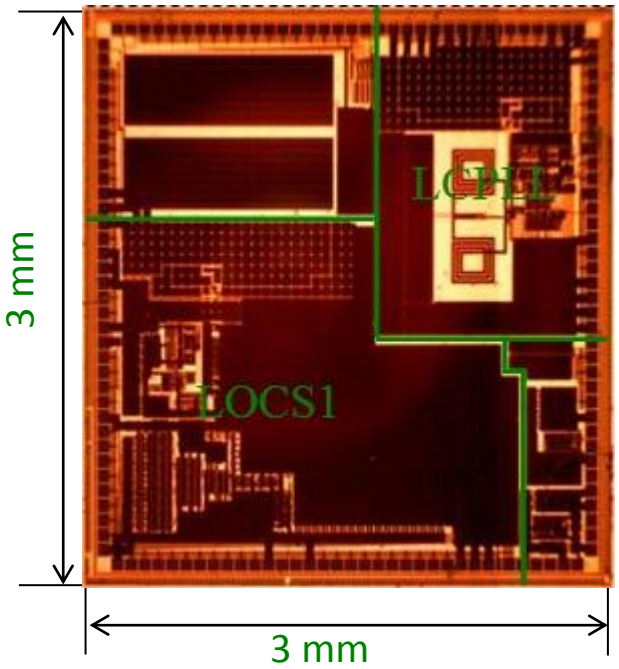
- Serdes-embedded FPGAs as receiving side benefits from the Versatile Link common project: optical interface and system design.

- Most challenging part: serializer, a 6-lane array serializer with redundancy switches at 10 Gbps.

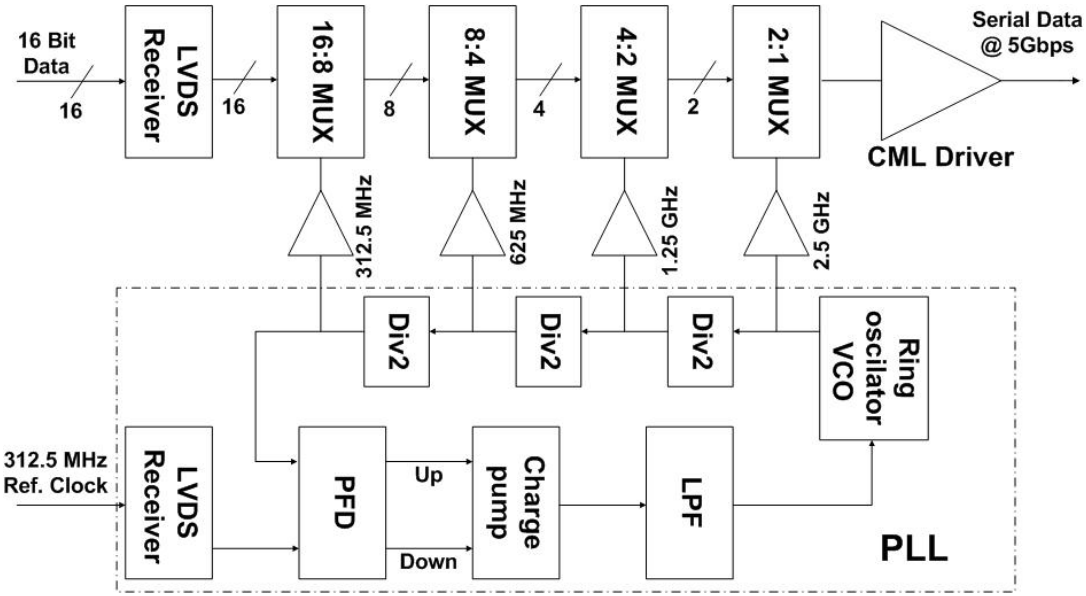
Jingbo Ye (Southern Methodist U, Tx)

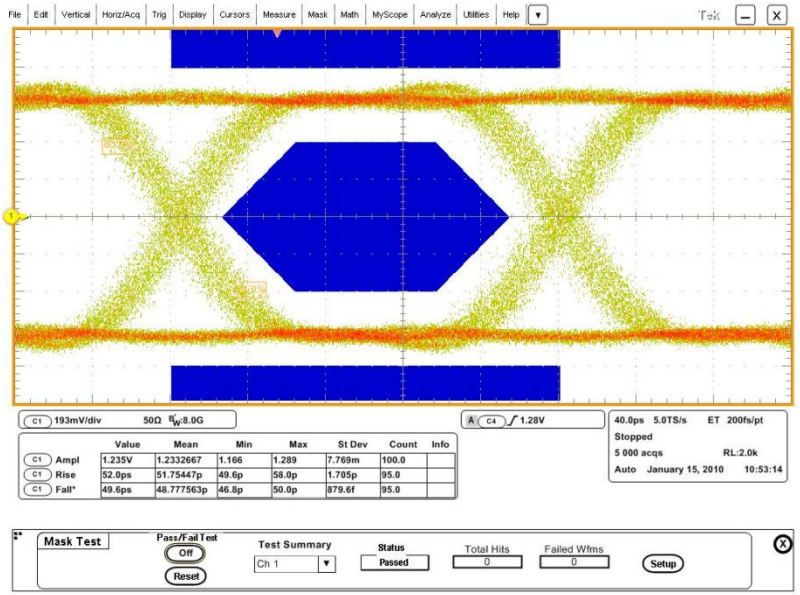
LOC1 Serializer ASIC

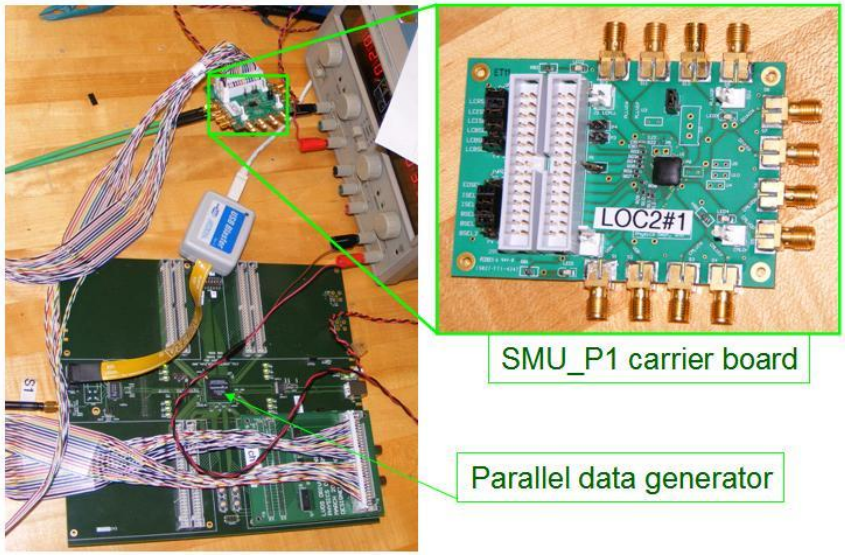
- Serializer:
- Prototype chip submitted August 2009.
- 3 × 3 mm2 comprising
  - LOCs1, a 5 Gbps 16:1 serializer.
  - LCPLL, a 5 GHz LC VCO based phase locked loop.
  - A CML driver
  - A divide-by-16 circuit.
  - Varactor, Voltage controlled capacitor.
  - SRAM block

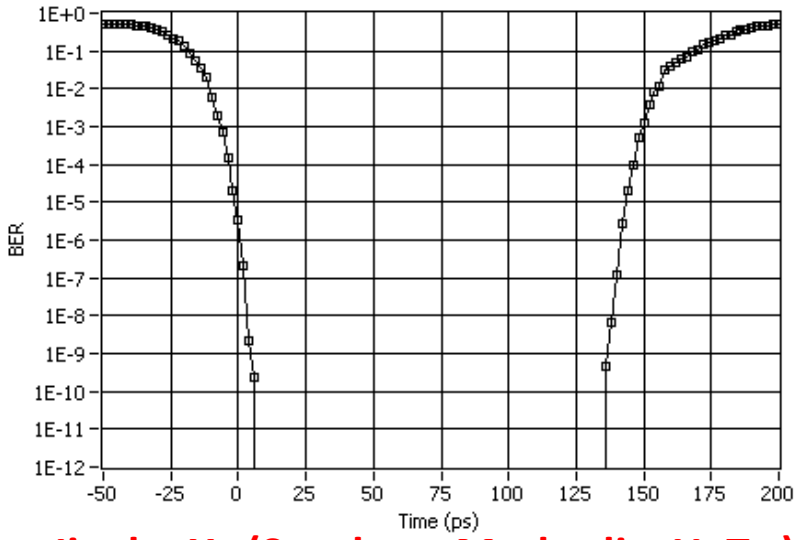


Test results of LOCs1



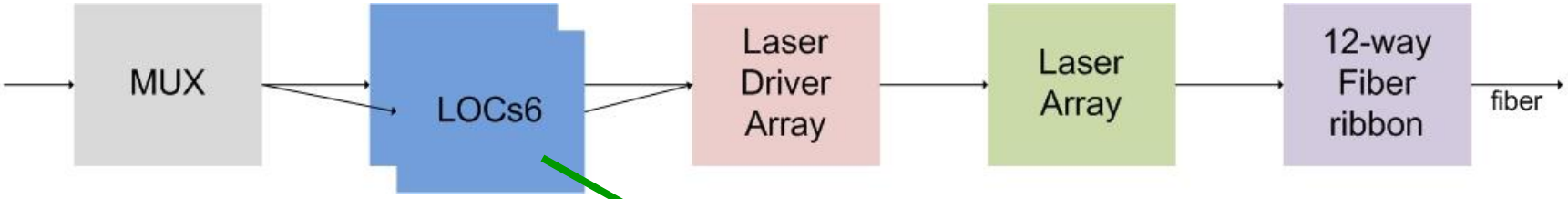




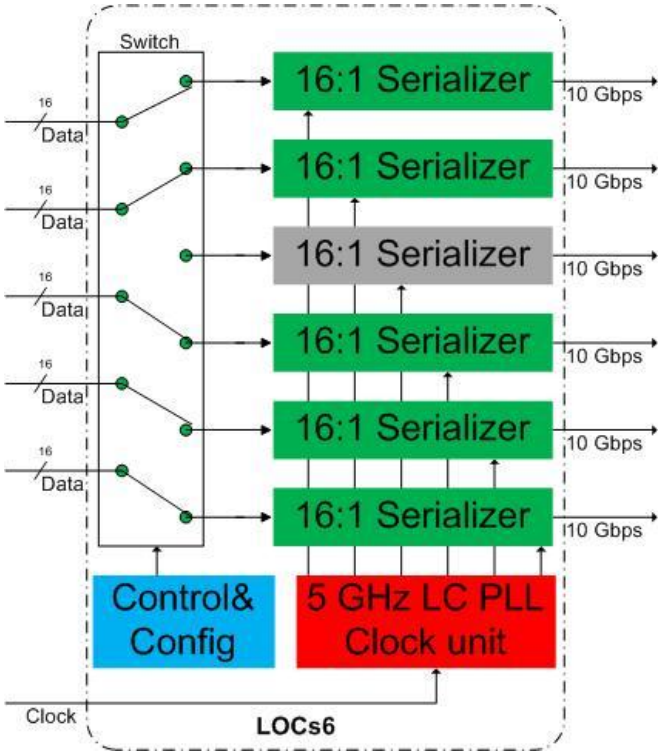


Jingbo Ye (Southern Methodist U, Tx)

Next version ASIC — LOCs6



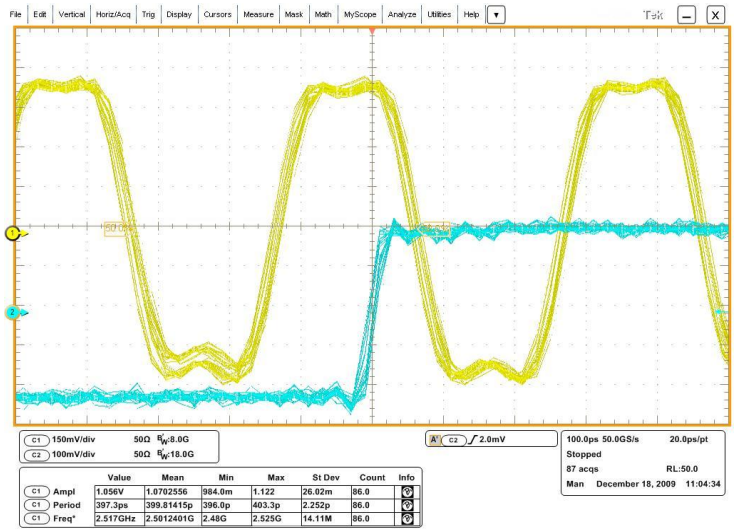
- Plan to use 2 LOCs6 chips with a 12-way fiber ribbon per FEB.
- Each chip has an array of six 16:1 serializers, each running at 10 Gbps.
- One of the six serializers can be configured as a redundant channel.
- The clock unit will be shared by the serializers to reduce the power.



5 GHz LC PLL

Fabricated in the same die as LOCs1 is a 5 GHz LC PLL

- **Tuning range: 4.7 to 5 GHz.**
  - Expected: 3.79 to 5.01 GHz.
  - Cause traced to the divider in PLL and will fix in the next design.
- **Power consumption: 121 mW**
  - Compare: Ring oscillator based PLL, 173 mW at 2.5 GHz
- **Random jitter: 1 - 2.5 ps (RMS)**
- **Deterministic jitter:< 17 ps (pk-pk)**



output clock locks to input clock

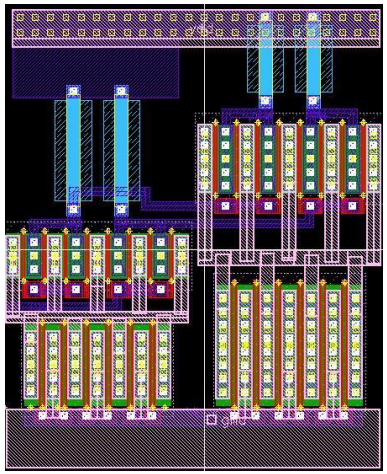
Jingbo Ye (Southern Methodist U, Tx)

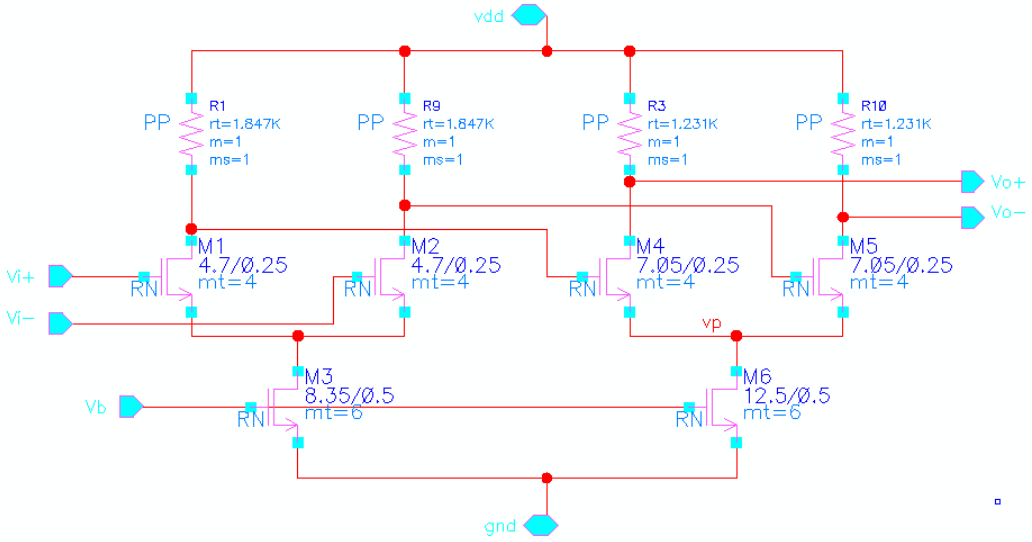
High speed CML circuit design

CML buffer for 5 GHz clock fan-out.
More CML circuit components ongoing.

Parameters for the CML buffer:

- Swing > 200 mV
- Frequ > 5 GHz
- Power: ~8 mW
- Two stage design
- Fan out two identical buffer without signal attenuation





Schematic and Layout

Jingbo Ye (Southern Methodist U, Tx)

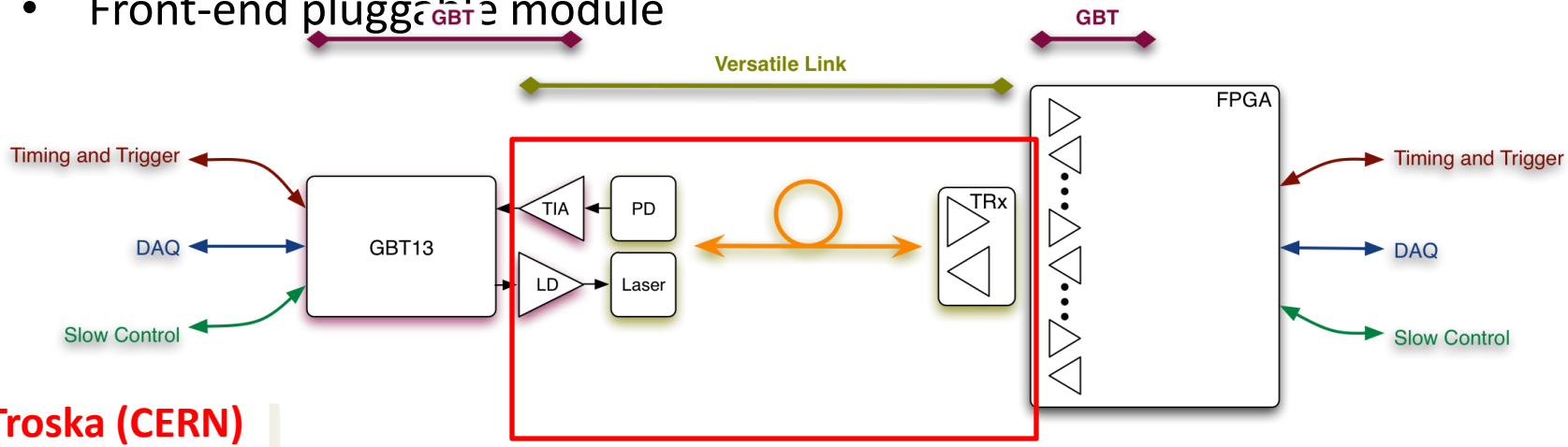
Plans and Summary

- Design of LOCs6
- As of the LOC1 tests, more needed.
  - More tests on LOCs1 are still needed
  - First proton test on LOCs1 produced very good results.
  - More tests may be needed to study SEE.
- Would like to investigate an array laser driver, LOCLD6
- Limited by manpower and resource. Need help in the development of the 100 Gbps/board system.

Versatile Link Project

- Optical Physical layer linking front- to back-end
- Bidirectional, ~5Gbps
- Versatile
  - Multimode (850nm) and Singlemode (1310nm) versions
  - Point to Point and Point to Multipoint architectures
- Front-end pluggable module

- Joint Project Proposal submitted to ATLAS & CMS upgrade steering groups in 2007 and endorsed in 2008
- Kick-off mtg in April 2008
  - Phase I: Proof of Concept *(18mo)*
  - **Phase II: Feasibility Study *(18mo)***
  - Phase III: Pre-prodn. readiness *(18mo)*

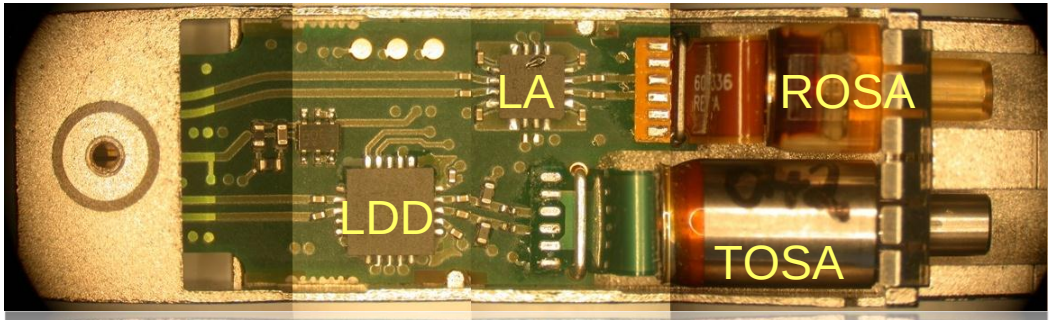


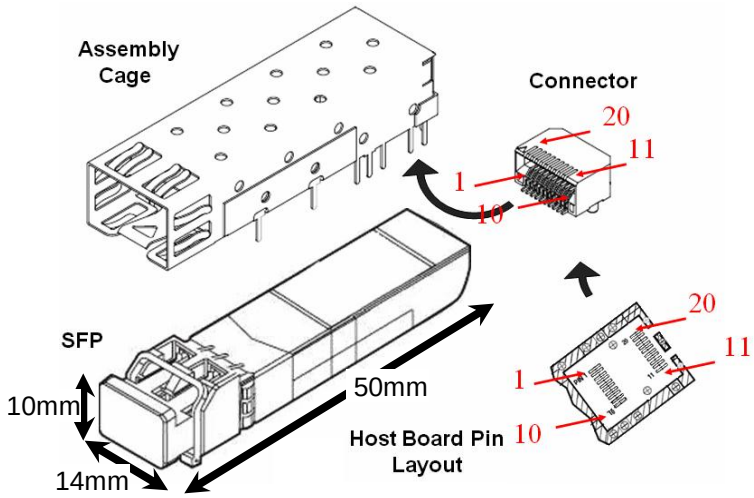
Jan Troska (CERN)

On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

VTRx packaging overview





- Based upon commercial SFP+ standard for 10G transceivers
- ASICs
  - Laser Driver (LDD) - GBLD
  - TIA - GBTIA
  - LA - not foreseen (inc. in GBTIA)
  - No microcontroller
- TOSA - Rad Hard Laser
- ROSA - Rad Hard PIN + GBTIA
- Keep Std. SFP+ Host board connector
  - No cage, alternate fixing T.B.D.
- Remove/replace material from std. SFP+ housing
  - Must test EMI tolerance and emission

VTRx

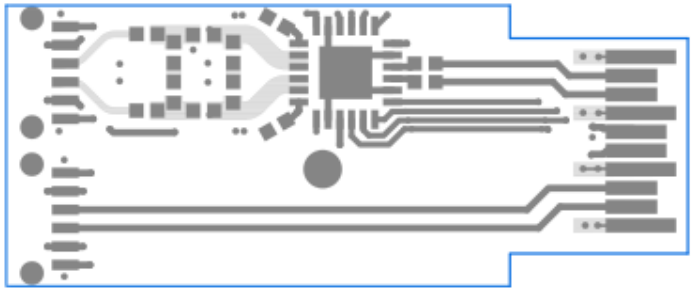
Components	Pkg know-how
GBLD	*Commercial Eval Boards*
GBTIA	*In-house Test boards*
Commercial LDD	*Industrial partnership*
Commercial TIA/LA	*VTRx prototype board*
ROSAs 850/1310nm	
TOSAs 850/1310nm	
Device modelling	

Jan Troska (CERN)

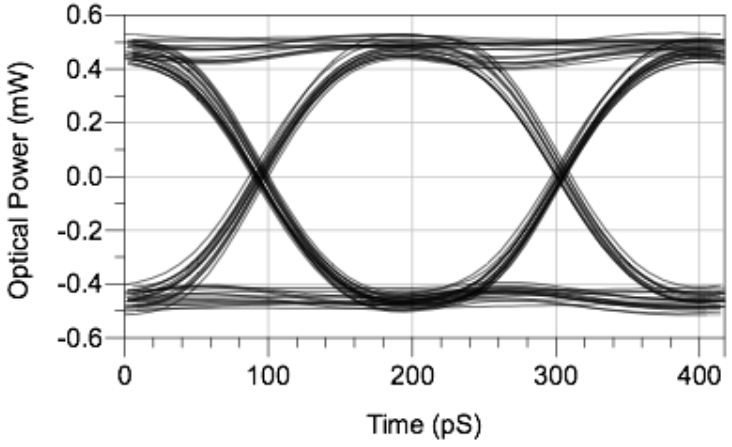
VTRx PCB design

Versatile Link

- Based upon experience gained with commercial ASIC evaluation boards and our own versions of such boards, have built our own SFP+ size-compatible test PCB housing:
  - Commercial edge-emitting laser driver
  - Commercial TOSA
  - GBTIA-ROSA



- PCB circuit simulations including the laser model were carried out to confirm the correct functionality of the board
  - Including optimization of the bias/matching network

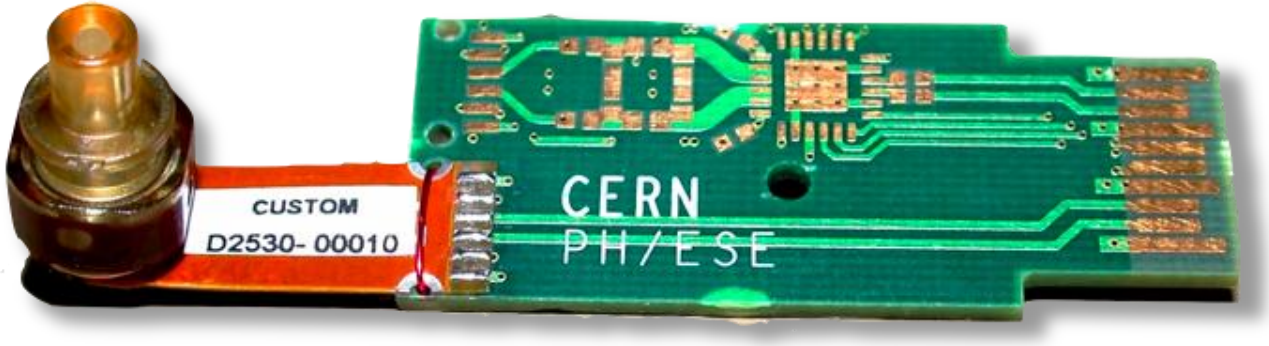


Jan Troska (CERN)

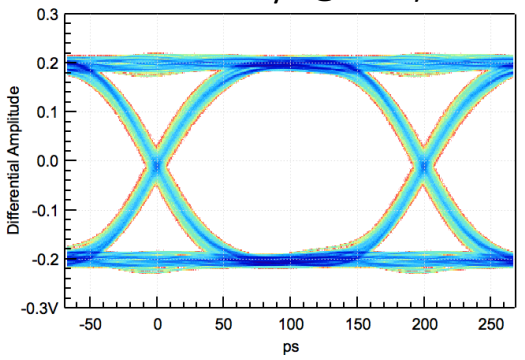
TOSA/ROSA integration on VTRx

Versatile Link

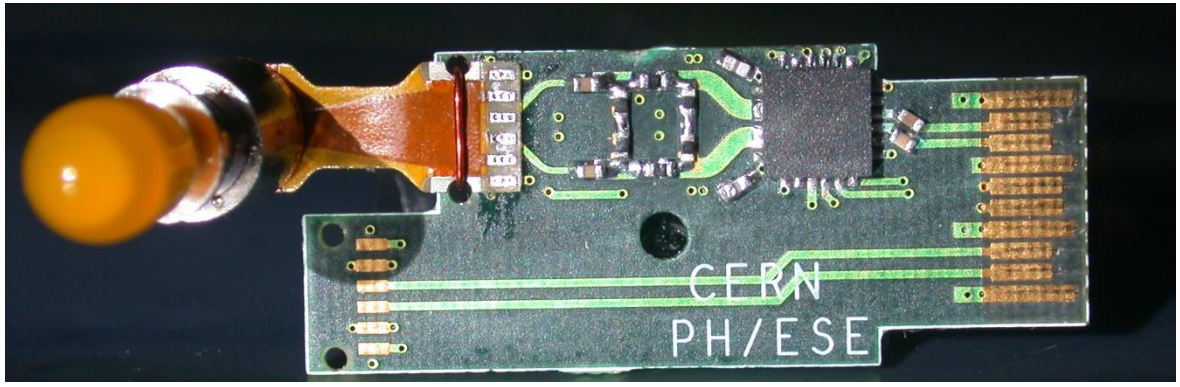
- GBTIA-ROSA on prototype VTRx PCB



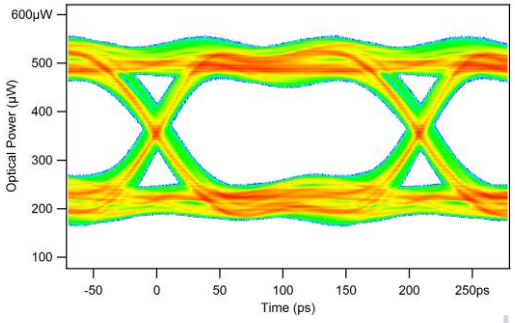
RX electrical eye @ 5 Gb/s



- TOSA and commercial Laser Driver on VTRx PCB



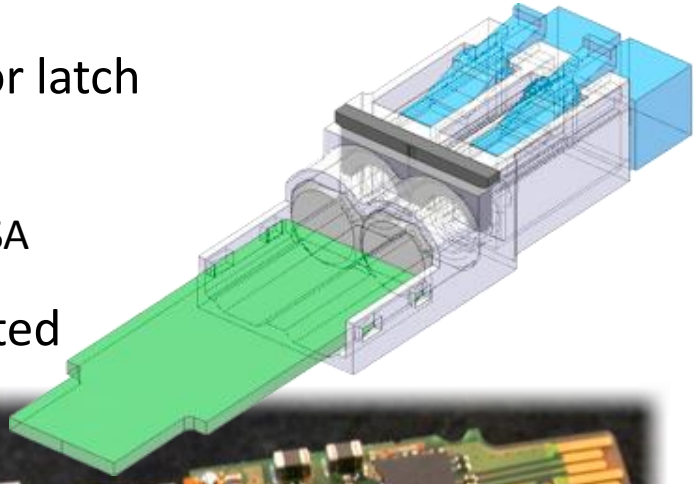
TX optical eye @ 4.8 Gb/s

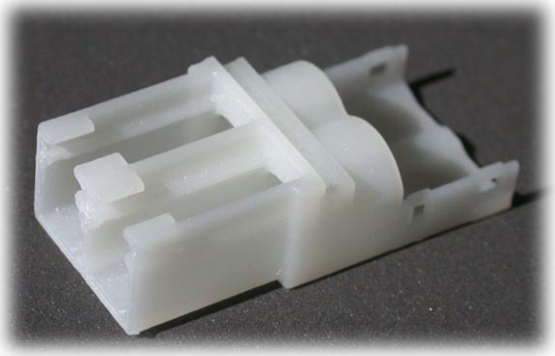


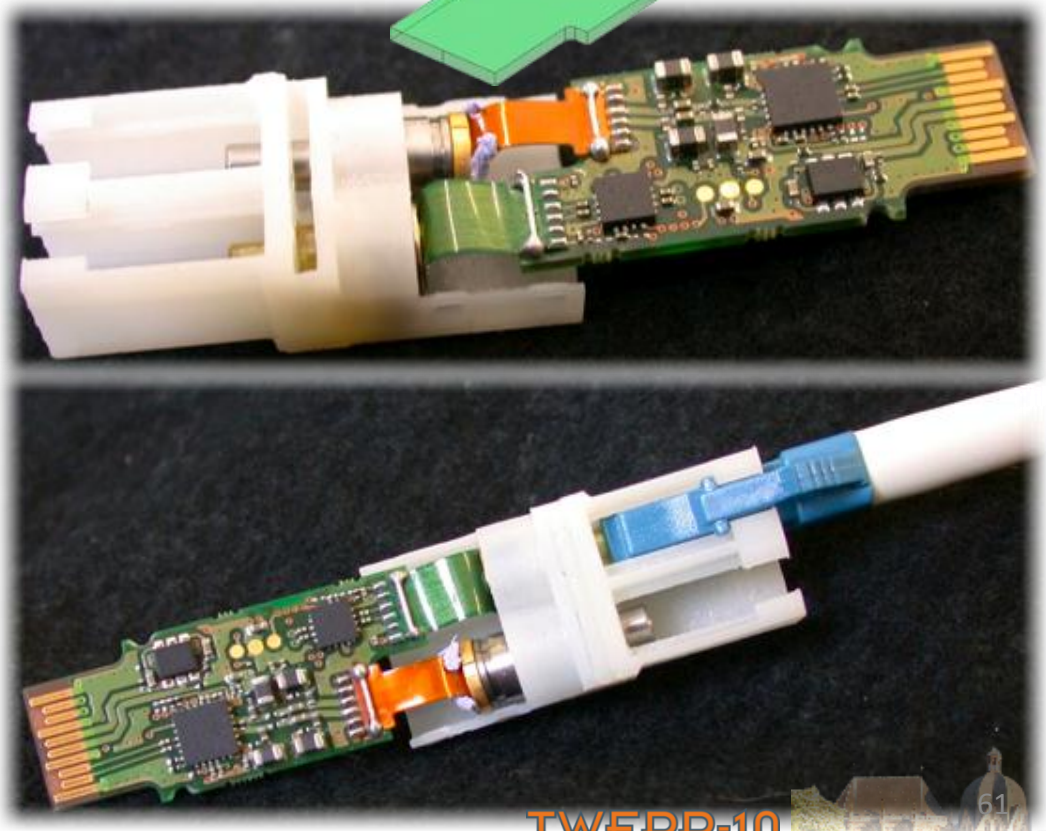
VTRx low-mass latch design

Versatile Link

- Working on mechanical design of VTRx connector latch to reduce overall mass of the transceiver
  - Part mechanically associates connector and TOSA/ROSA
- Rapid prototype plastic samples successfully tested





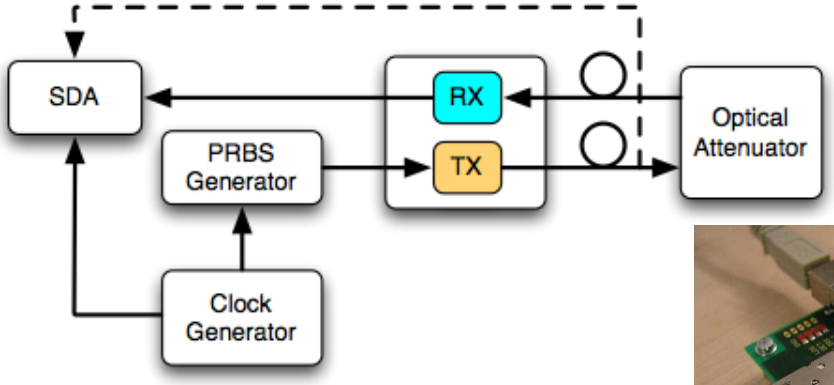


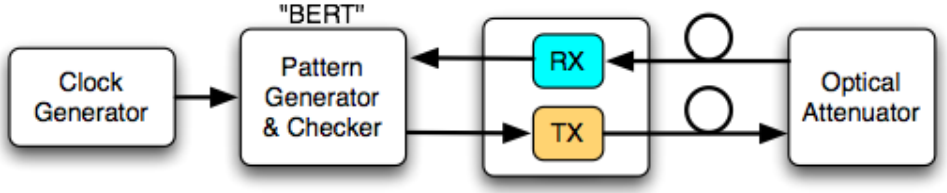
Jan Troska (CERN)

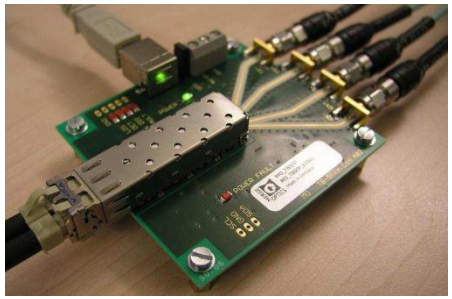
Functionality Testing Overview

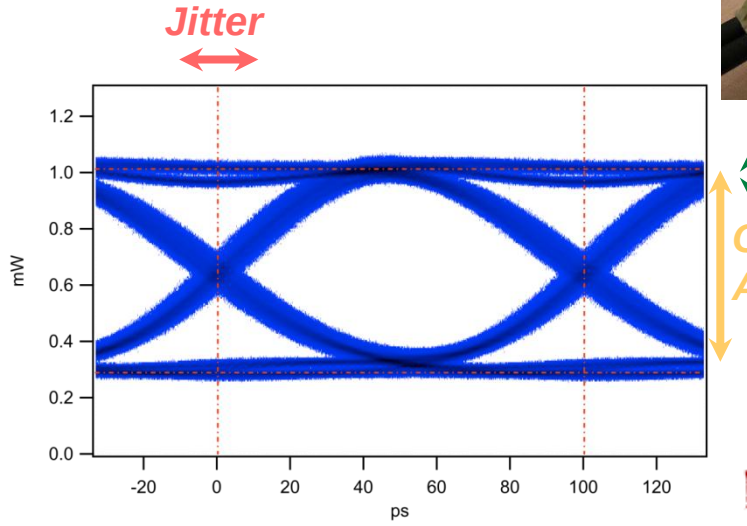
Versatile Link

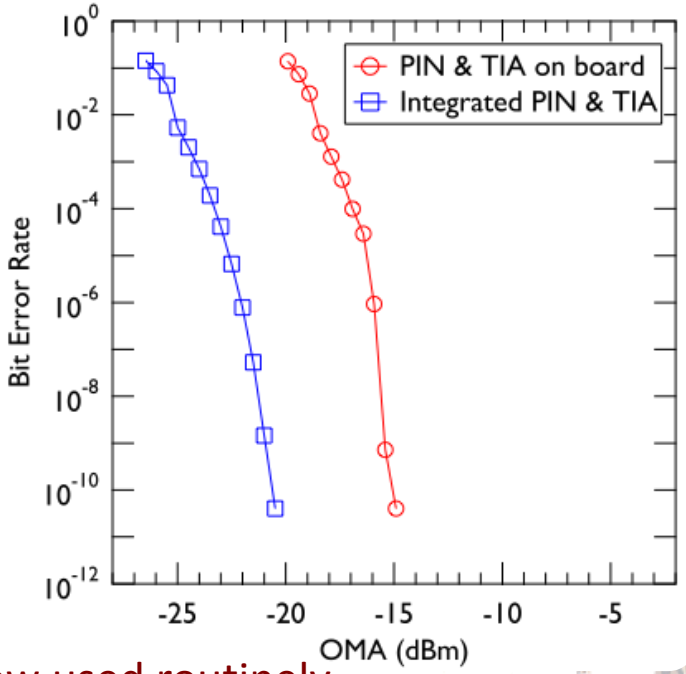
1. Signal "Eye" Diagrams - optical for TX, electrical for RX
2. Bit Error Test (BERT)









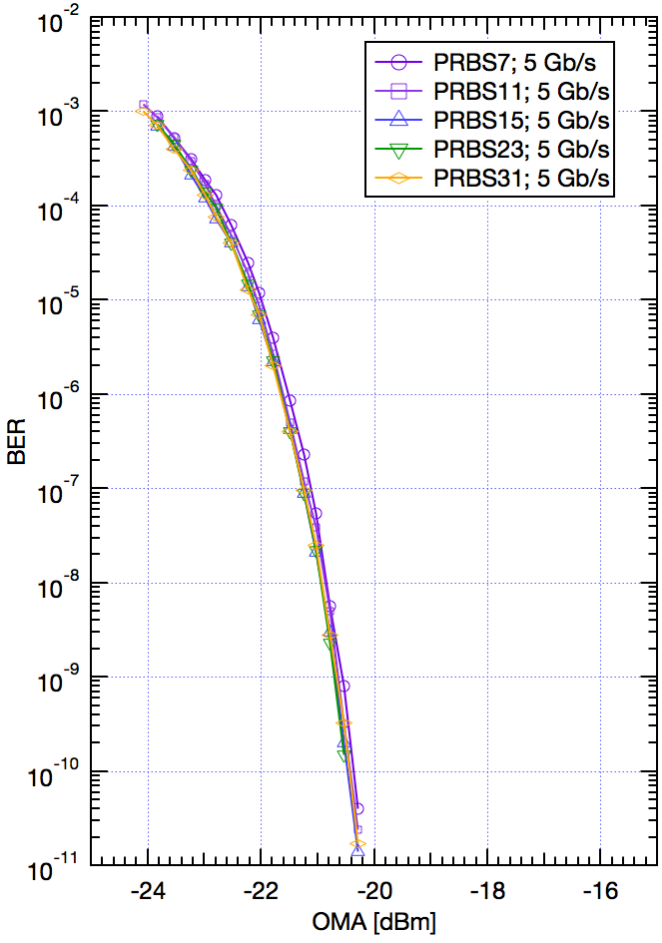


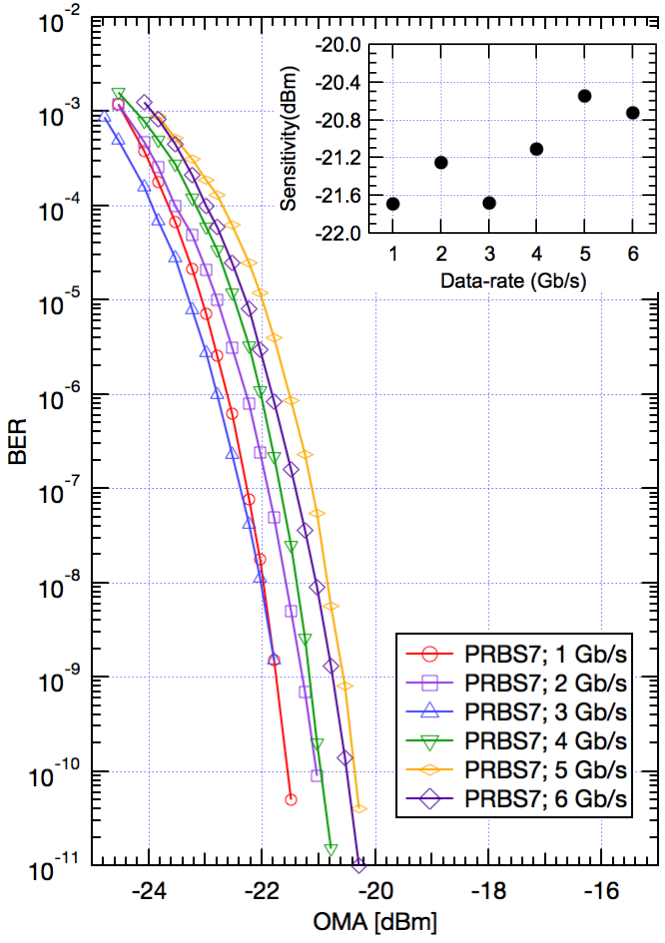
Jan Troska (CERN)

Test Methods now used routinely

GBTIA ReceiverOSA performance

- Evaluate impact of data-rate and pattern length on GBTIA ROSA sensitivity

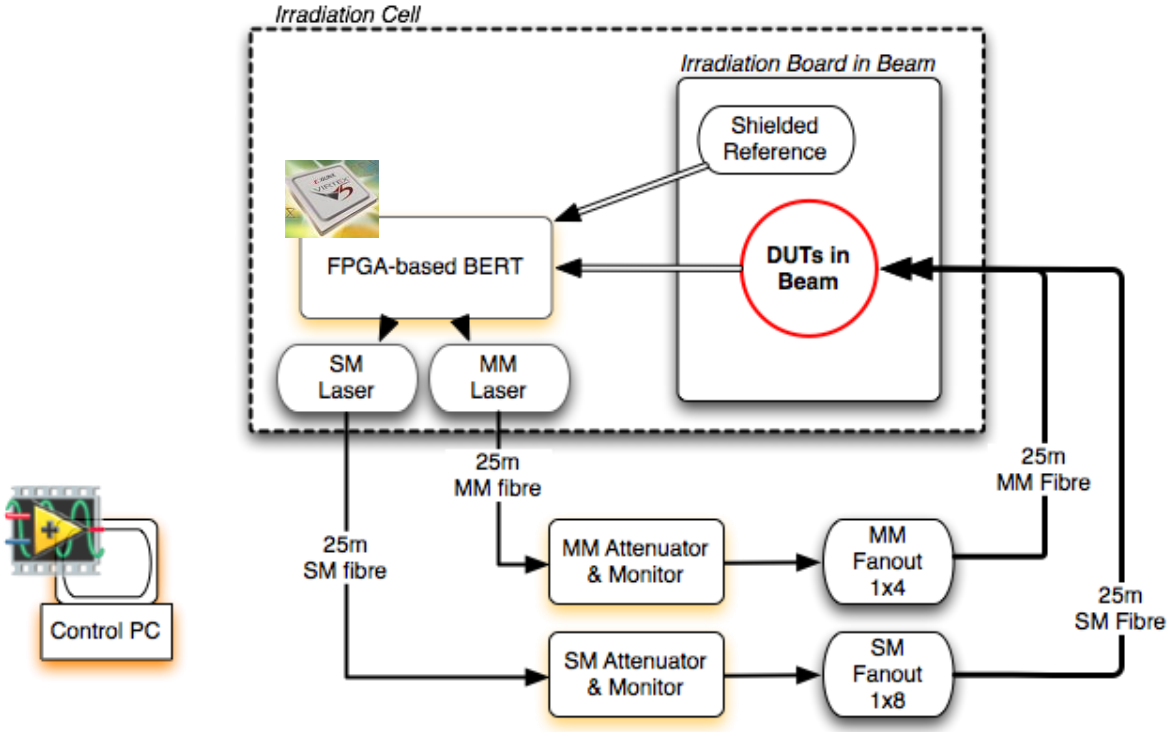




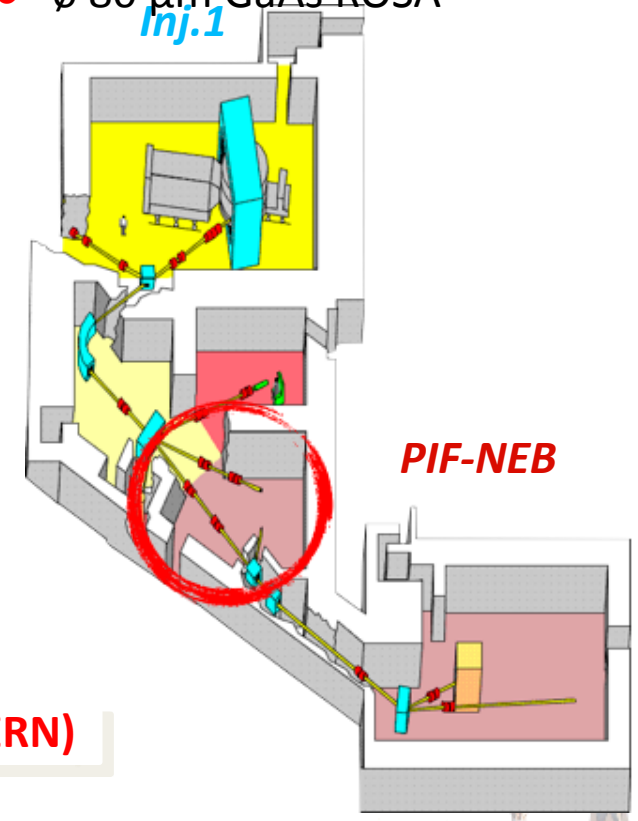
- Favourable comparison to bare-die tests
  - ROSA pkg not detrimental to functionality
- No pattern length sensitivity
- Expected reduction in sensitivity with data-rate
  - Acceptable magnitude

Jan Troska (CERN)

PSI Proton SEU Test



- 62.91 MeV p+ beam
- 1-4x10^8 p/cm^2/s
- ø 60 µm InGaAs PIN and GBTIA ROSA
- ø 80 µm GaAs ROSA



- Cross-check previous burst-error results & test GBTIA SEU immunity
- Xilinx Virtex-5 based BERT
  - Six channels, 2 Gb/s to 6 Gb/s
  - GBT encoding inc. FEC, Error logging
- Labview-based instrument control

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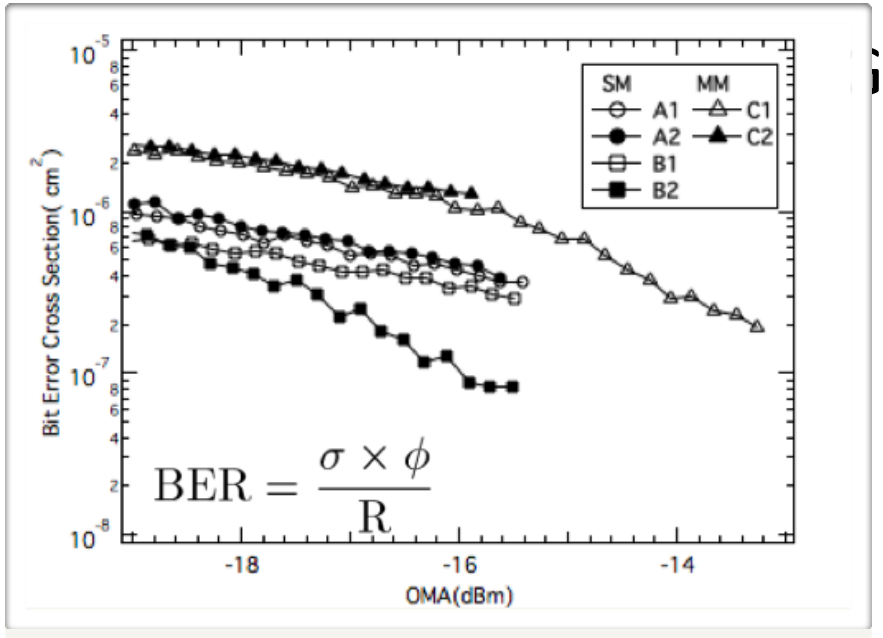
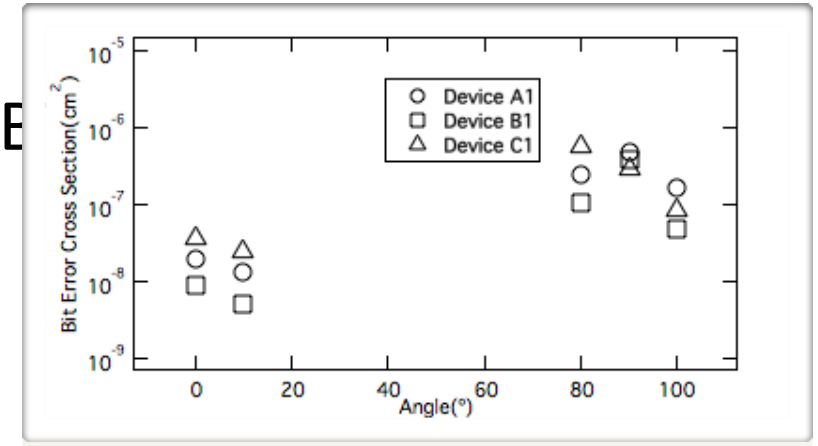
SEU test result preview (1/2)

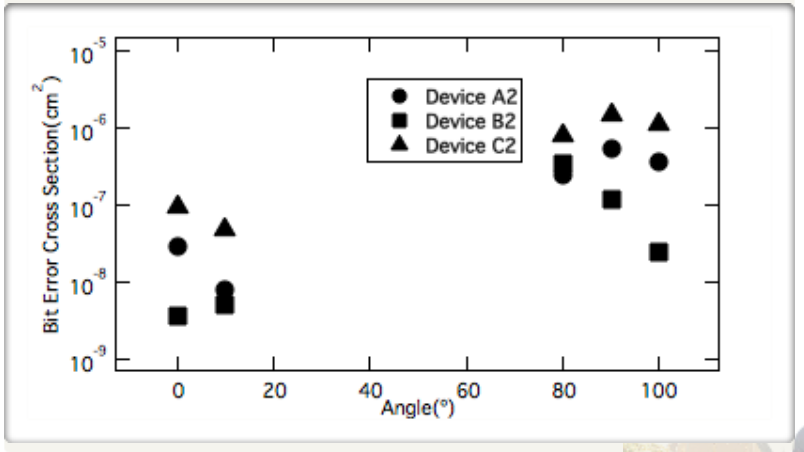
Versatile Link

– Similar overall trend but several orders of magnitude difference in response between devices

- SM PINs A1 and A2, GBTIA ROSA B1 and B2, MM ROSA C1 and C2







Bit Error Cross Section as a function of the incidence angle,
90 == grazing incidence
0 == normal incidence

Results for near grazing incidence @ 3Gbps

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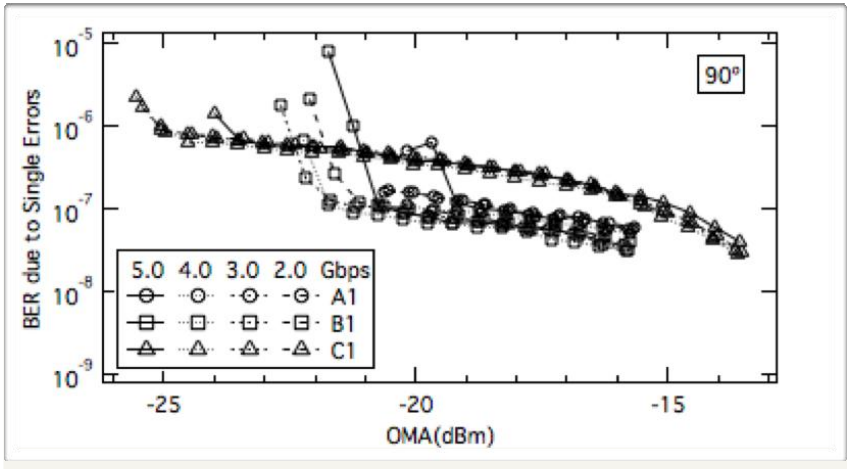
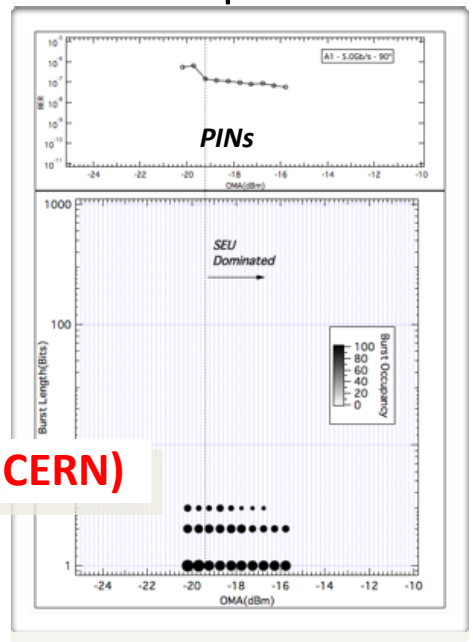
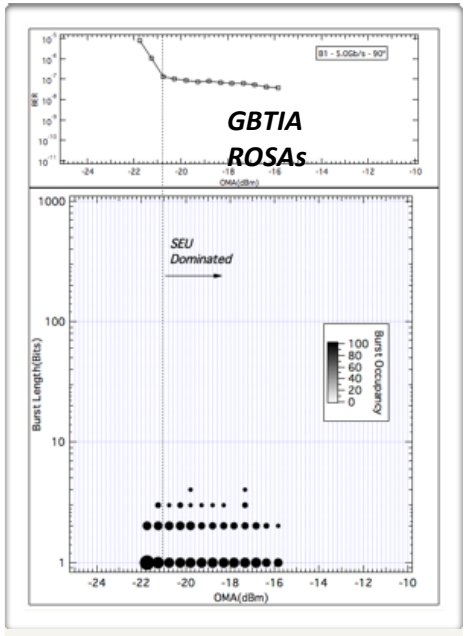
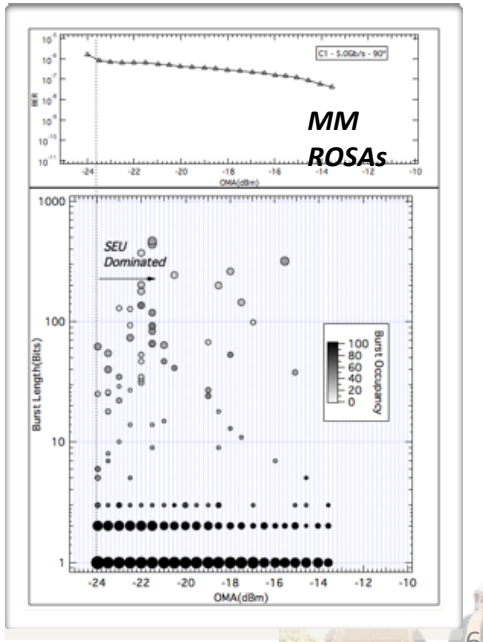
SEU test result preview (2/2)

- BER due to single bit flips is similar for all devices
- BER is independent of data rate within the range of investigation
- Burst lengths limited in PINs and GBTIA ROSAs
- Longer bursts seen in ROSAs with unshielded amplifiers









Jan Troska (CERN)

Summary & future work

- In terms of our Phase II deliverables
  - Specifications for on-detector components
    - Available and under discussion within Versatile link project, soon to be distributed more widely
  - Packaging
    - In-house development of both PCB and mechanical pkg progressing well
    - Successful integration of GBTIA and PIN into ROSA
      - Detailed measurements of multiple devices in near future
    - Defining strategy for future variants (GBLD, TOSA types)
  - Functional test methods applied to testing of transmitters and receivers
    - Excellent performance of GBTIA ROSA
    - Performance limitation of current VTRx design being studied in simulation
  - Radiation Testing
    - SEU test results compare well with previous results
      - Burst errors not observed in GBTIA or high-speed commercial TIA
    - Pion test carried out, lots of data to analyse

xTCA
Micro/Advanced Telecommunications Computing Architecture

LHCb Upgrade

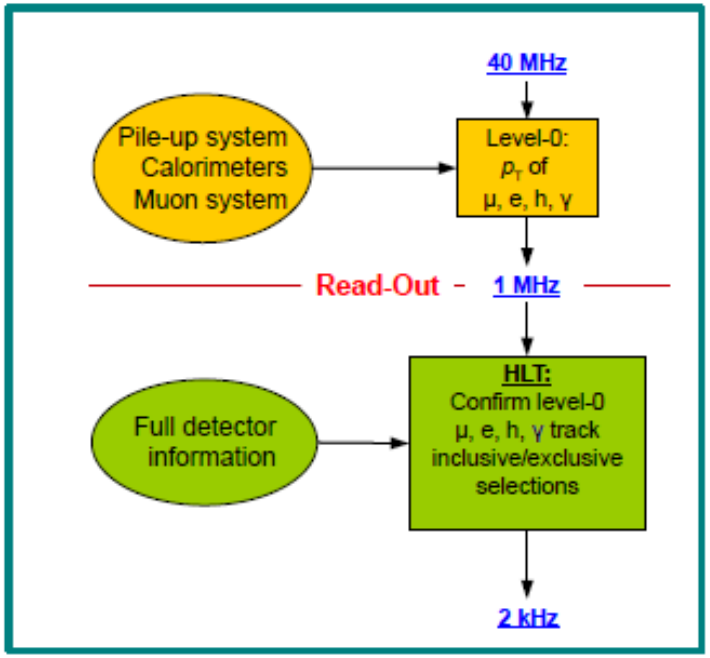
Outline

- LHCb Upgrade
- Building blocks for high speed read-out
- Performances
- Slow control
- Scalable read-out architectures

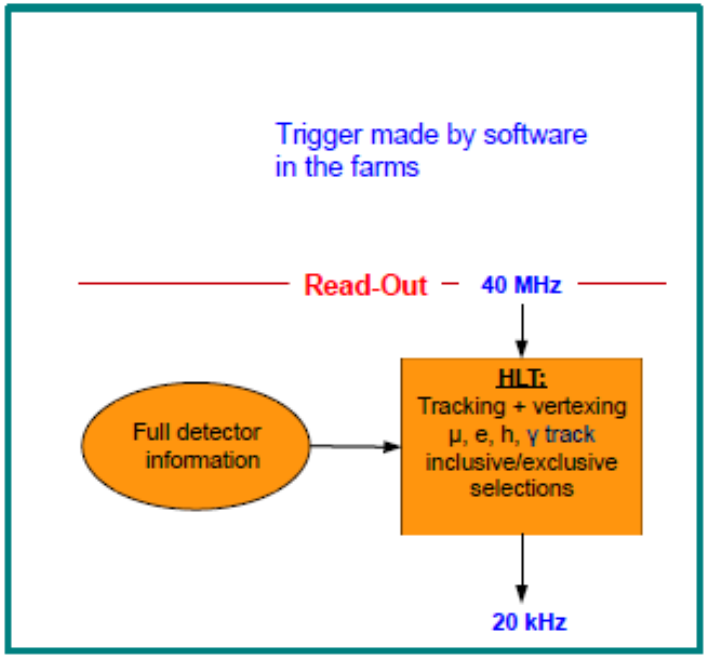
J-P Cachemiche, CPP Marseille

40 MHz Front-end readout

Trigger upgrade



Current trigger scheme



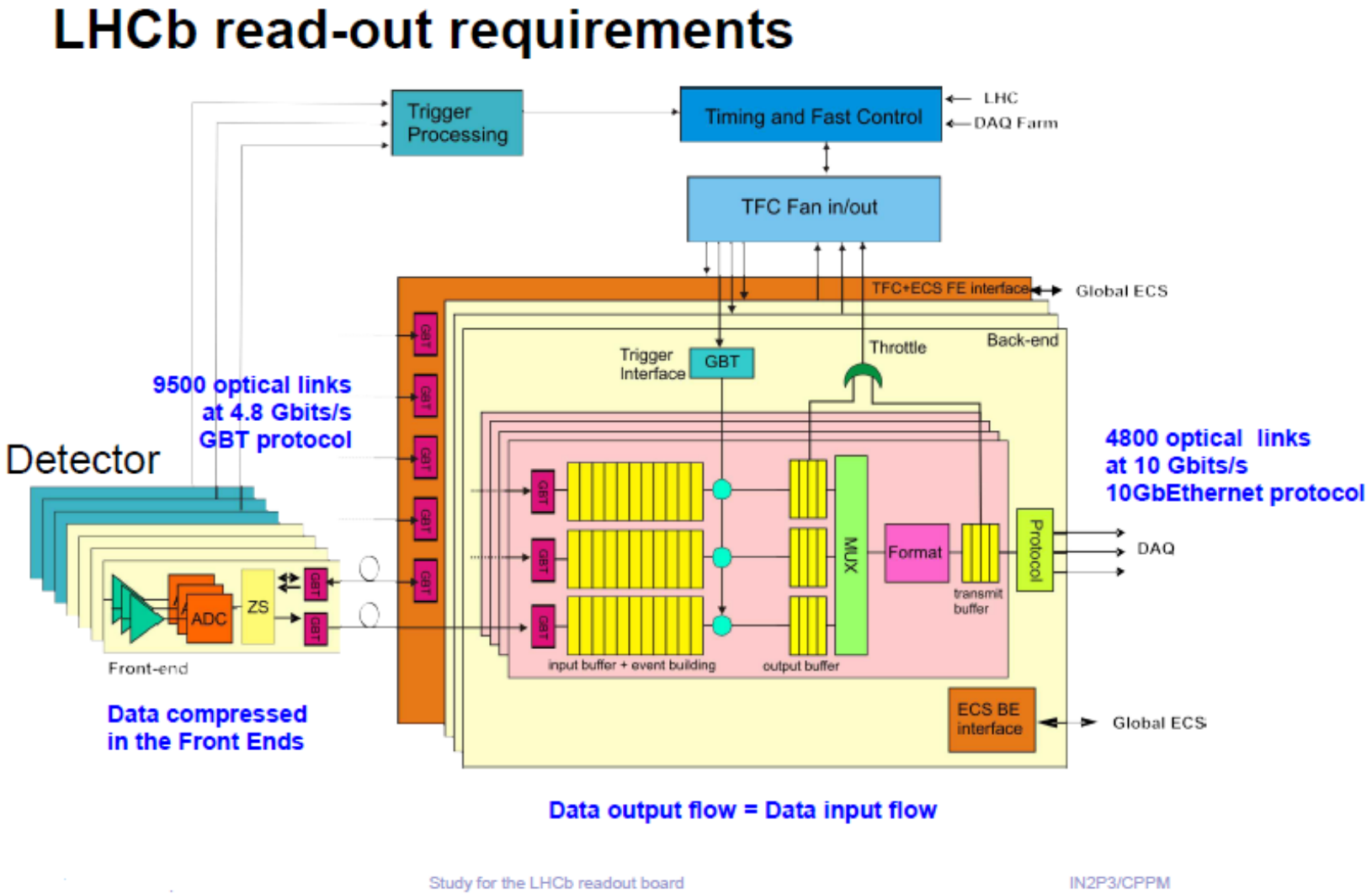
Future trigger scheme

All detectors read at 40 MHz

Study for the LHCb readout board IN2P3/CPPM

J-P Cachemiche, CPP Marseille

40 MHz Front-end readout



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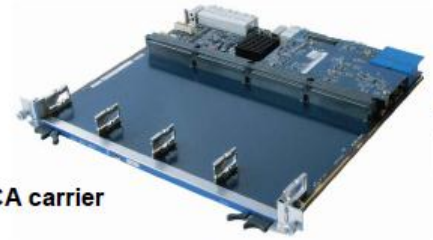
μ/ATCA

Development based on xTCA



ATCA carrier

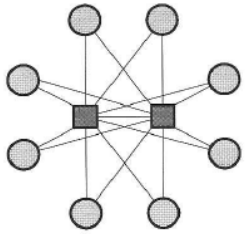
ATCA

μTCA

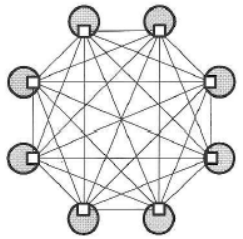
AMC card

TWEPP 22 September 2010 Study for the LHCb readout board IN2P3/CPPM

Powerful connectivity in xTCA standards



Dual star topology



Full mesh topology

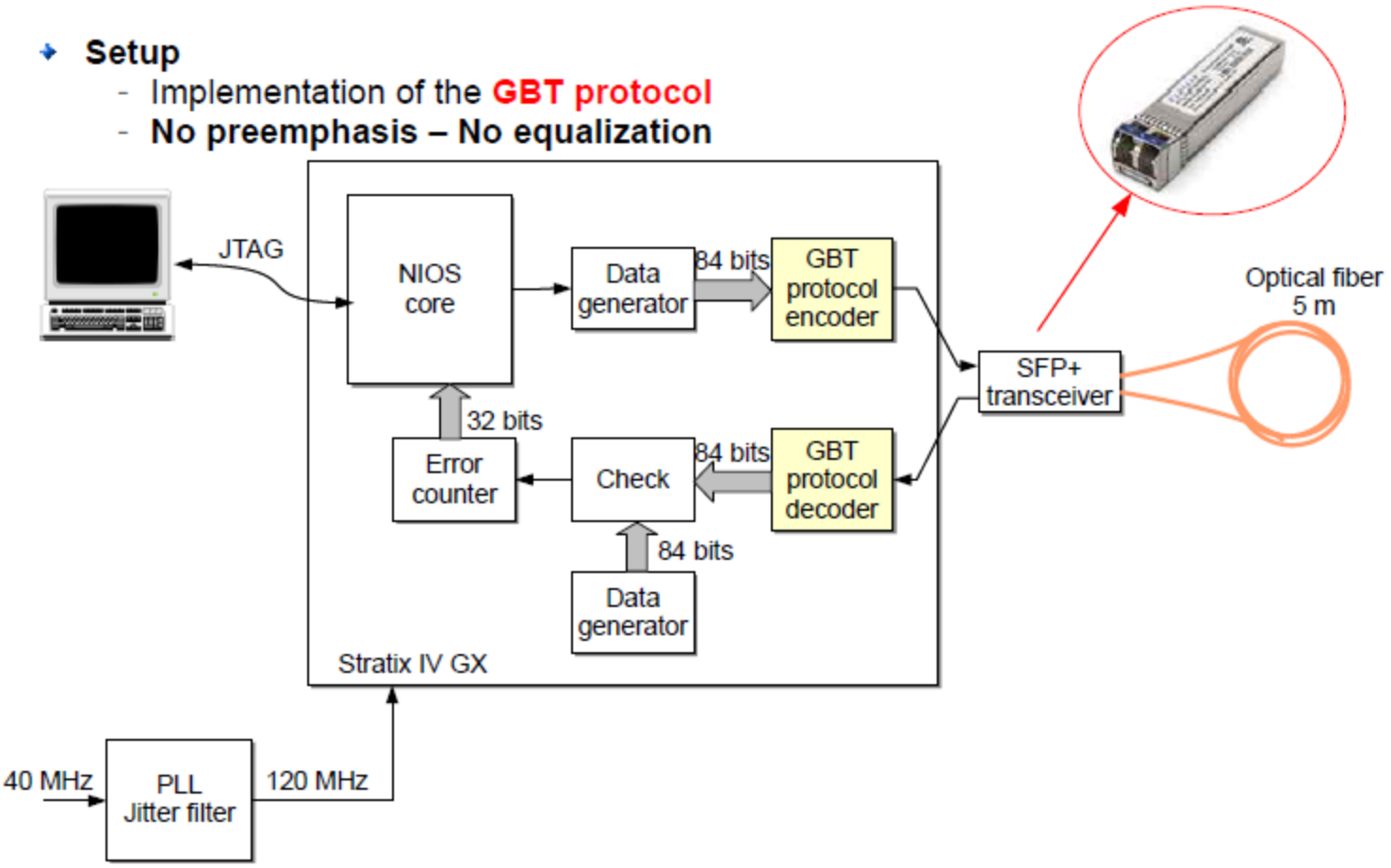
Study for the LHCb readout board IN2P3/CPPM

J-P Cachemiche, CPP Marseille

Serial I/O

Serial lines at 8 Gbits/s

- **Setup**
  - Implementation of the **GBT protocol**
  - **No preemphasis – No equalization**



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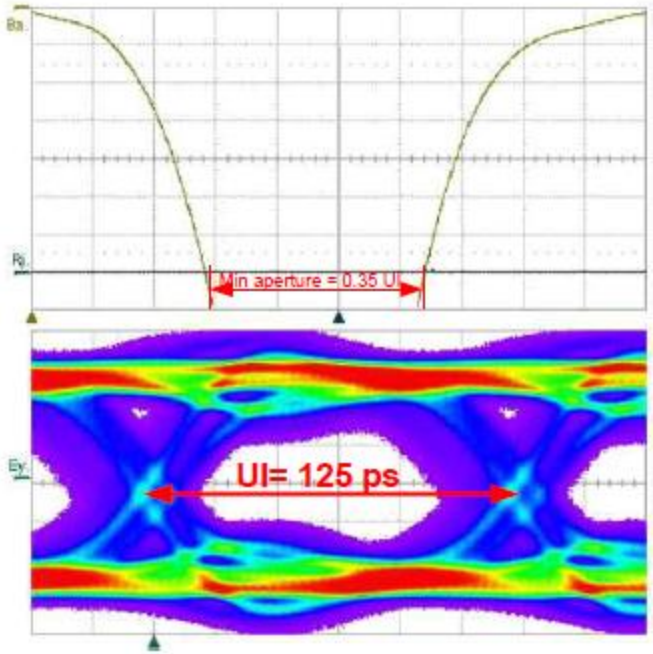
Serial I/O

Measurements at 8 Gbits/s

Serial link at 8 Gbits/s with GBT protocol



- **Measured jitter at 10^{-12}**
  Total : **77 ps (p to p)**
  Random : **3.0 ps**
  Deterministic : **36 ps**
- **Estimated error rate :**
  10^{-15} without pre-emphasis or equalization
- Closure of eye diagram: inter symbol interference due to attenuation of high frequencies

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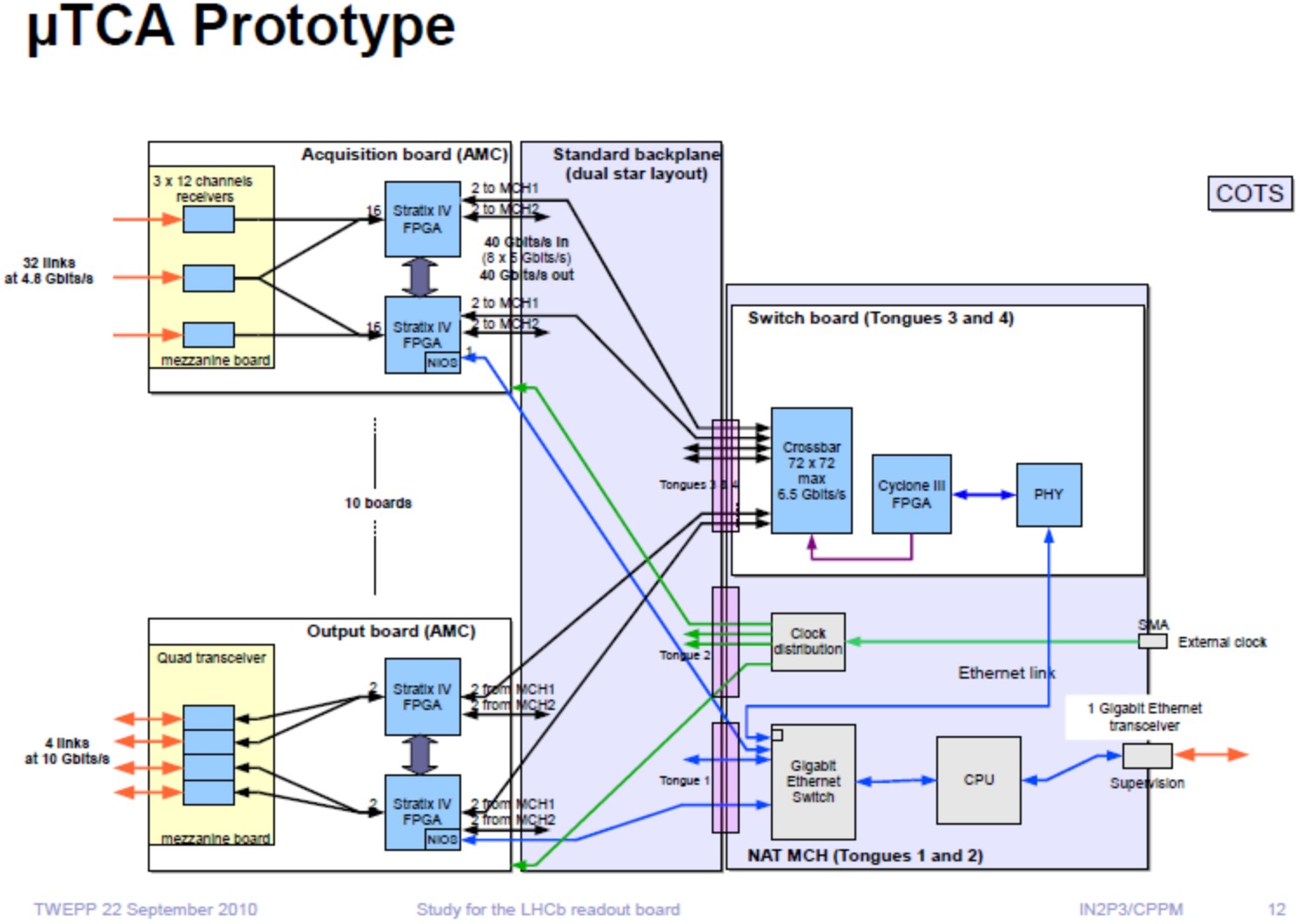
Full μTCA prototype



J-P Cachemiche, CPP Marseille

Conclusions

- Study on signal integrity is on-going
  - Serial links at 4.8 and 8.5 Gbits/s are OK
  - Pre-emphasis and equalization should allow to increase speed up to 10 Gigabit/s
  - New version of the board with Stratix GT running at 10 Gbits/s soon available.
- xTCA system can be used to build scalable architectures for LHCb upgrade
  - Advantages of a standard: mechanics, COTS systems, interoperability, ...
  - Star topologies present in the standard might help for time distribution, slow control and communications between boards.
- Mezzanine concept allows flexible reconfiguration of boards
  - Quick redesign at low cost
- Supervision system based on NIOS cores embedded in FPGAs is very promizing

Study for the LHCb readout board

J-P Cachemiche, CPP Marseille

A demonstrator for a level-1 trigger system based on µTCA technology and 5Gb/s optical links.

Greg Iles

Rob Frazier, Dave Newbold (Bristol University)

Costas Foudas*, Geoff Hall, Jad Marrouche, Andrew Rose (Imperial College)

20 September 2010

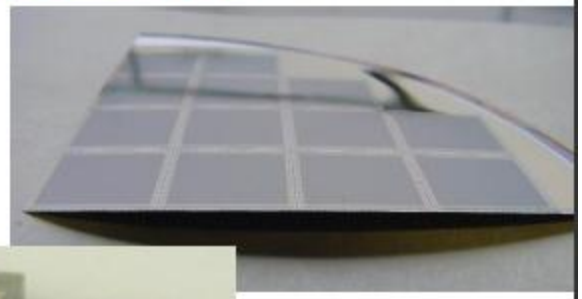
*** Recently moved to University Ioannina**

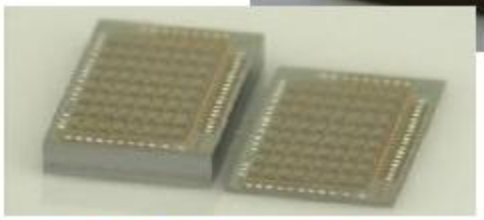
New Interconnect Technologies

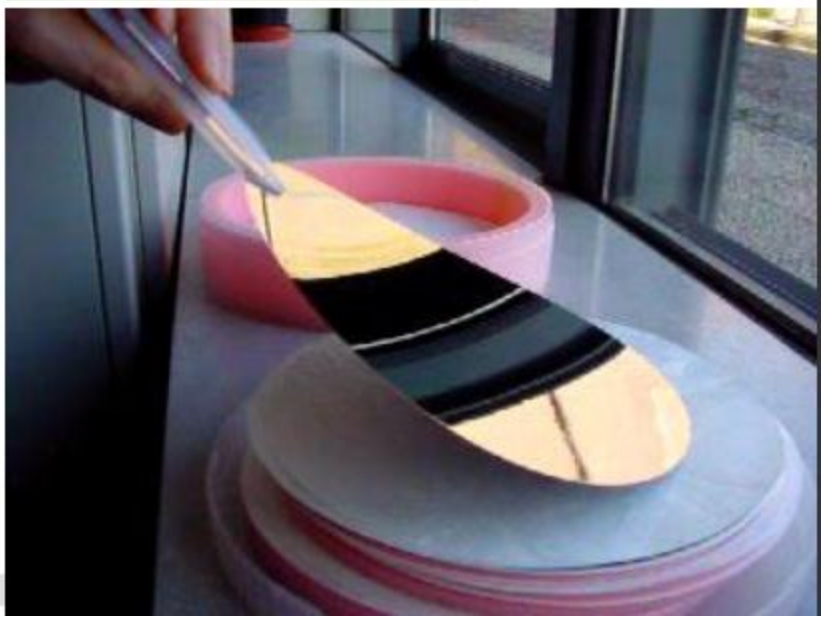
CCDs, Pixels

BACKSIDE ILLUMINATED IMAGERS: THINNING

- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers and temporary wafer (de-)bonding technology
- IMEC results:
  - Thinning down to 15 um
  - Total thickness variation ~ 2 um on 200 mm wafer







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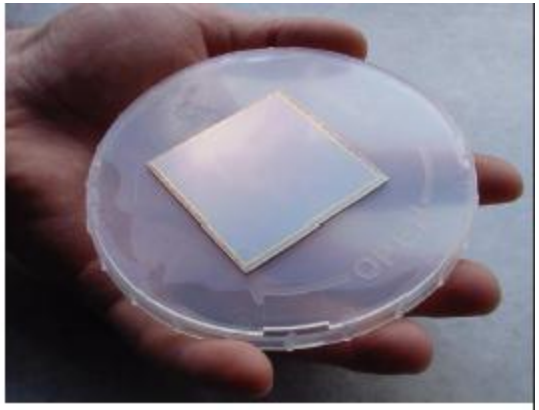
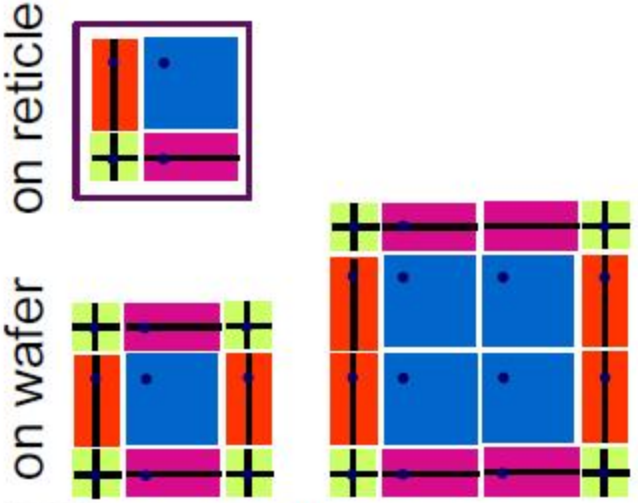
Piet De Moor (IMEC)

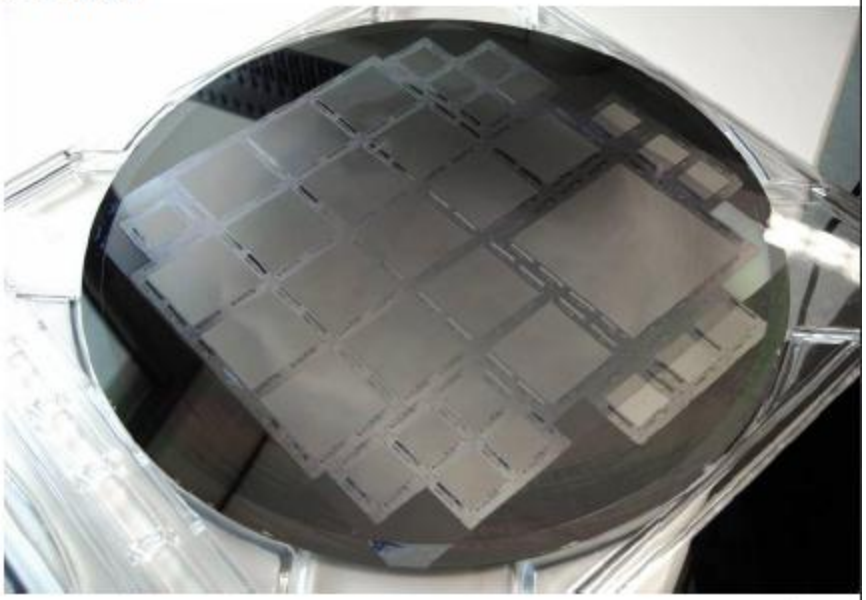
CCDs, Pixels

LARGE AREA IMAGERS: STITCHING

- Stitching allows large area imagers:
  - Up to 1 imager per wafer
- Different imager sizes on one wafer demonstrated:
  - 12x12 mm^2, 25x25 mm^2 and 50x50 mm^2
- Application: e.g. X-ray







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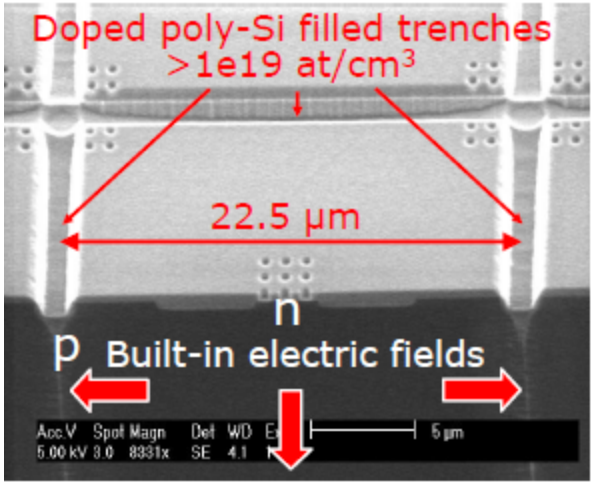
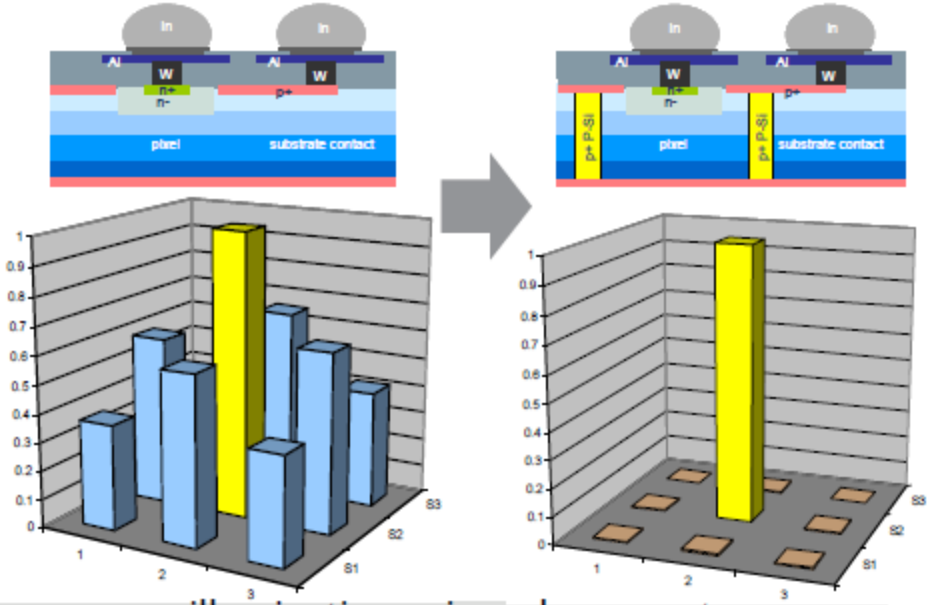
Piet De Moor (IMEC)

Imagers: Pixels Insulation

HYBRID BACKSIDE ILLUMINATED IMAGERS : TRENCHES FOR ZERO CROSS-TALK

- Poly-Si doped trenches separating pixels:
  - Disadvantage: (limited) reduction in fill-factor
  - Advantage: no cross-talk
- Demonstrated using laser point source
- ongoing optimization: recovery of good charge collection & QE/



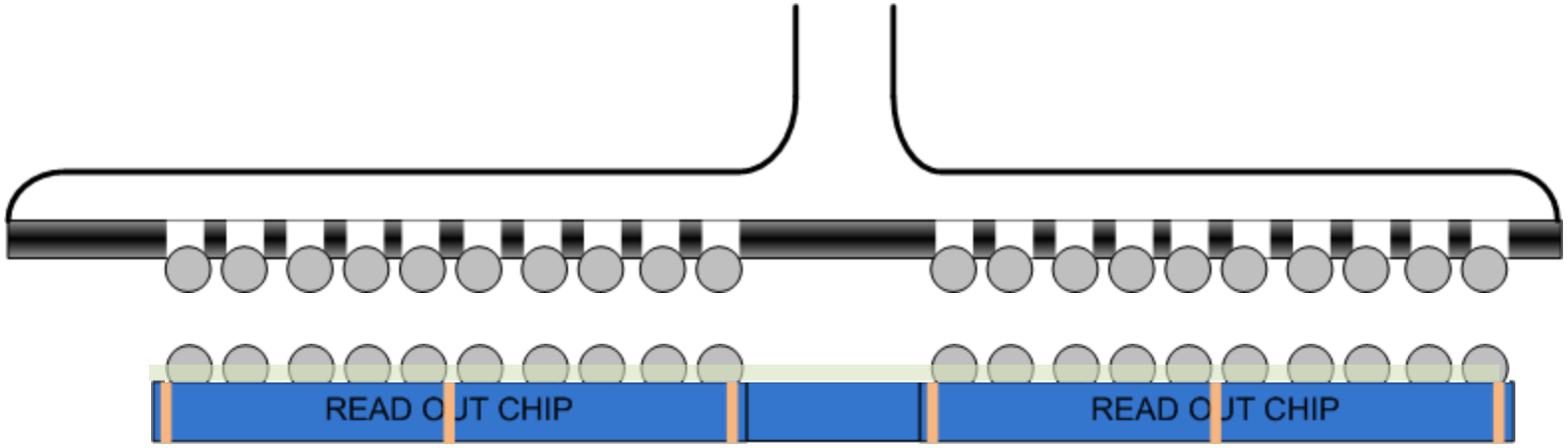


imec © IMEC 2010 PIET DE MOOR illumination using a laser spot 9

Piet De Moor (IMEC)

Solder Mass Transfer Process – “Gang Ball Placement”

- The ultimate low-cost solder ball placement process is the mass transfer of solder spheres on the whole wafer at the same time.
- Stencil grid with predefined holes and vacuum is used to lift the solder sphere.
- Solder bumping defects can be repaired with the singe solder ball placement systems
- Limited by ball size, minimum 60 µm at present therefore suitable for 100 mm pitch
- Pac Tech foresees 40 µm bumps coming in 1-2 years.

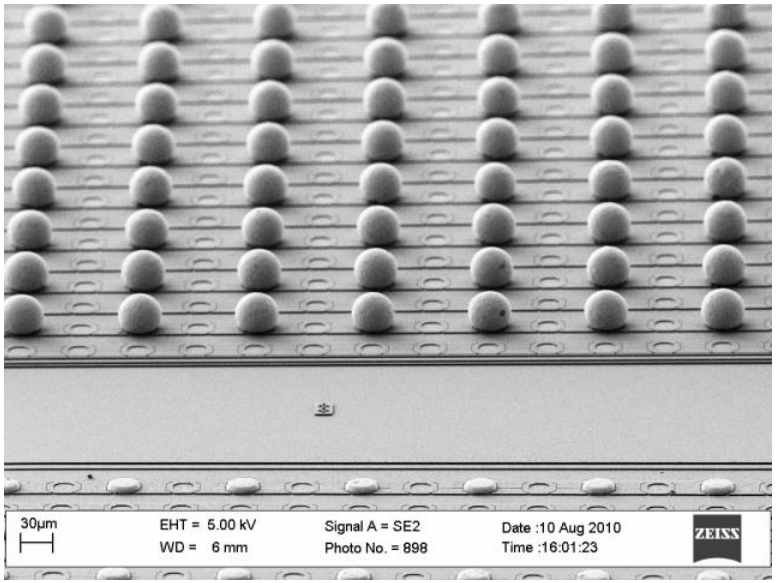


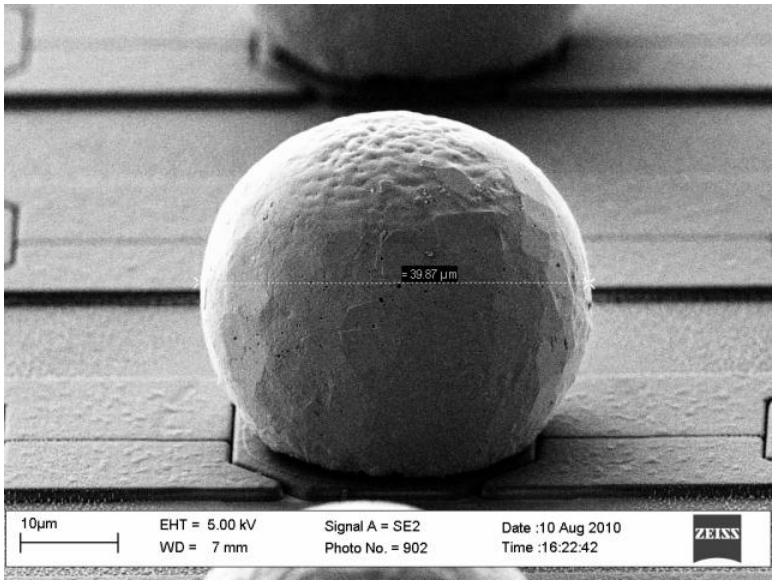
Solder mass transfer is very efficient process to attach the solder spheres to wafer

Bump-bonding

Solder Ball Placement Test

- 40 µm sized solder balls (very advanced) were jetted (spitting process) on a Timepix chips with ENEPIG UBM with 110 µm pitch at Pac Tech.
- Individual shear tests were done (30 bumps), giving an average shear force of 8 grams / bump (good results).
- Looking forward to do more SBB tests on Timepix chips





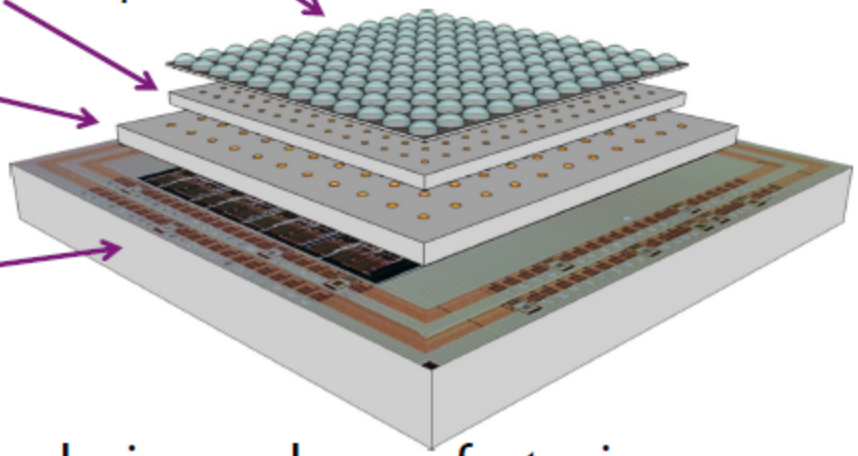
Sami Vaehaenen (CERN)

AREA 3D INTEGRATED IMAGERS

- Status: system architecture study of an

imaging system on a chip-stack

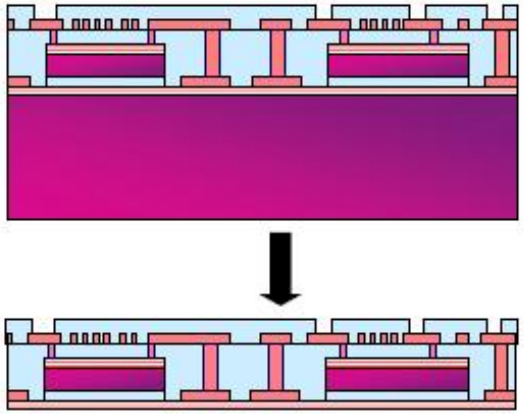
- Integration of micro-optics layer:
  - Ultra wide field of view
  - Filters for hyperspectral imaging
- Shared pixels = multiple pixels per bump
- Smart analog/digital read-out:
  - Ultra high dynamic range
  - ADC per group of pixels
  - Variable resolution (active binning)
- Smart digital processing:
  - 2D distributed group of processors
  - Face recognition

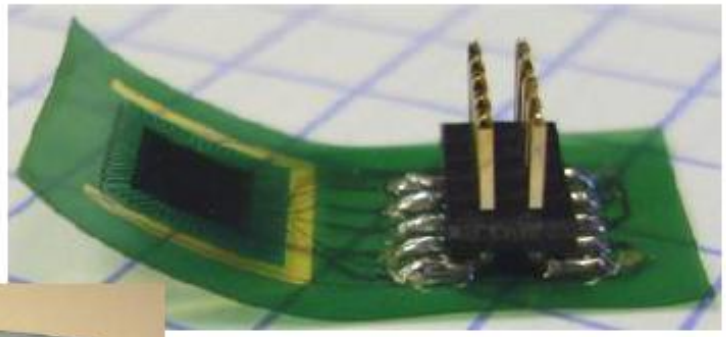


- Next step: demonstrator design and manufacturing

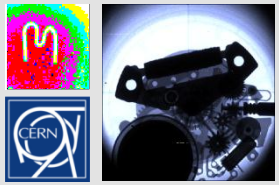
ADVANCED INTEGRATION: FLEX EMBEDDED IMAGER

- Technology:
  - Extreme wafer thinning (20 um)
  - Embedding on flex
- Example of related IMEC techno:
  - Functional microcontroller in flex substrate
- Embedding of tracking imager ongoing





Piet De Moor (IMEC)



CONCLUSIONS

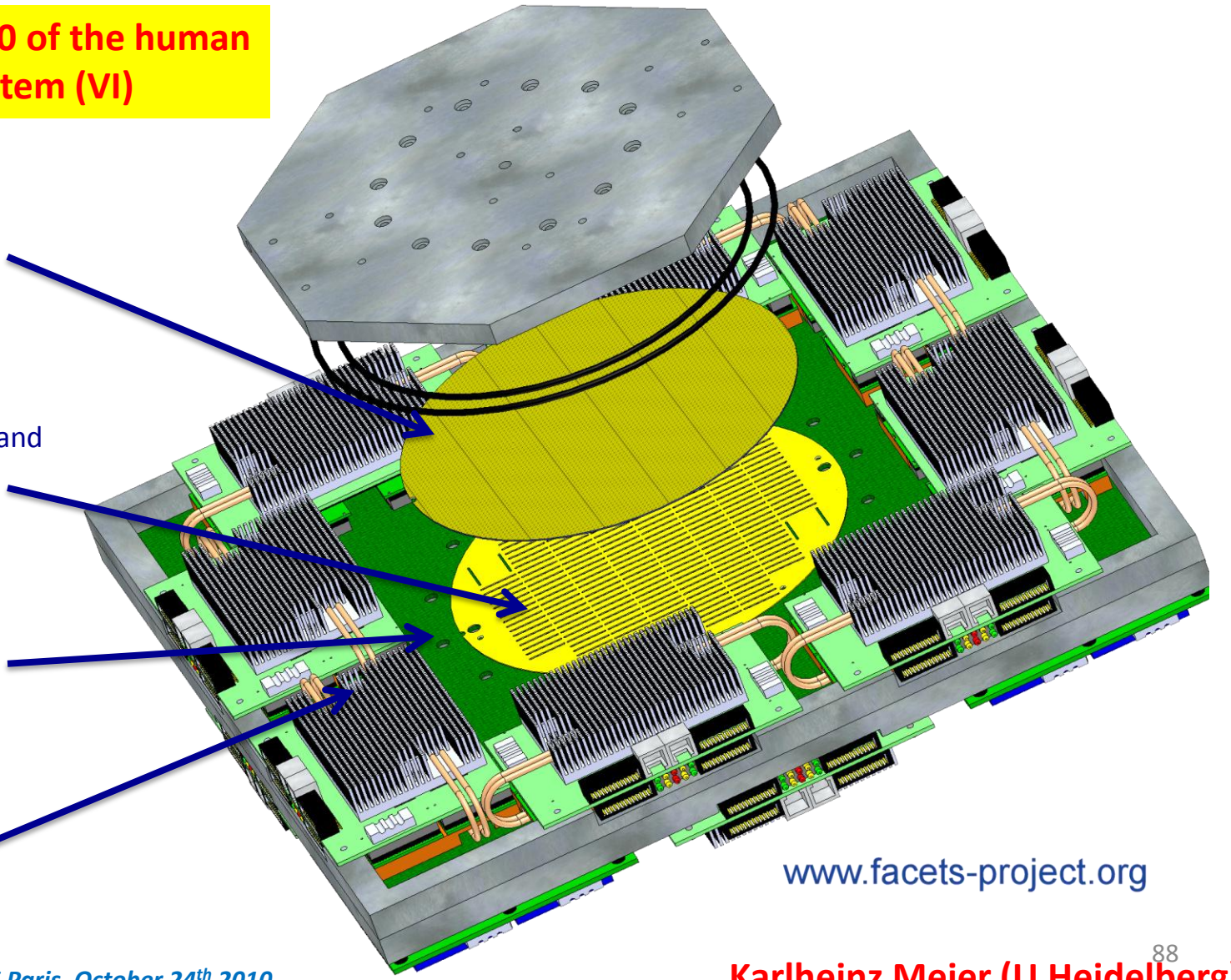
- Advanced 3D integration technology enables smart imagers with high performance
- The best integration scheme is application dependent
- imec has capabilities in:
  - Backside thinning and passivation
  - High density bumps
  - Through Si vias
  - Advanced assembly
- imec can offer specialty product development on demand up to small volume production (CMORE)

Piet De Moor (IMEC)

Parallel Computing

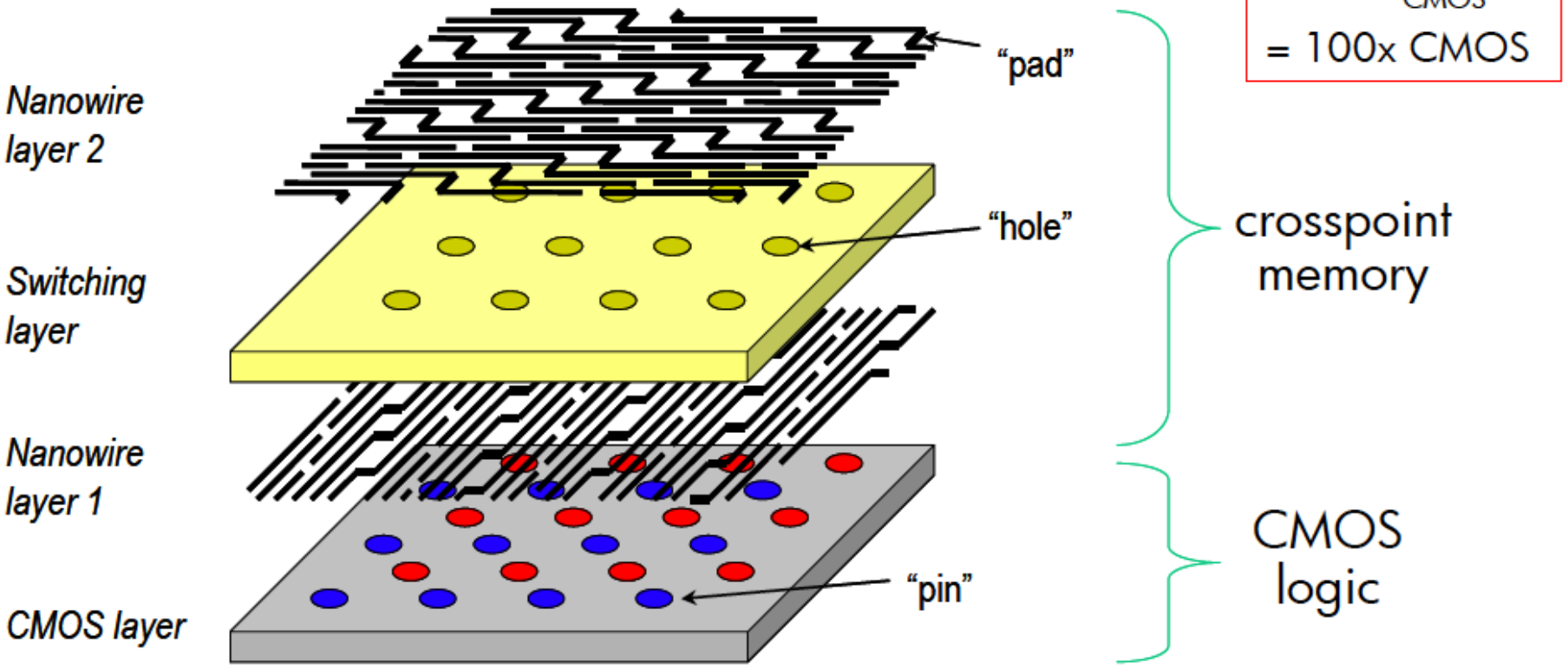
Neural Processing Unit, 200.000 Neurons, 50.000.000 Synapses Demonstrate self-organized, fault tolerant, low power, accelerated information processing (Heidelberg, BrainScales Consortium))

Approx. 1/10.000 of the human visual system (VI)



Karlheinz Meier (U Heidelberg)

HP FPNI : Field Programmable Nanowire Interconnect



Nano redundancy → defect tolerance
Small size, high yield → low cost
Low energy

G. Snider et al, IEEE Trans. Nano (2007)

Joining reliable CMOS and faulty nanoelectronics

Radiation Hardness

Radiation Hardening for Space Applications

- Dedicated processes for space are not affordable any more
- SOI is sometimes used
  - Low SEU rates, latch-up free, some concerns on TID
  - SOI is less readily available, analogue IPs need to be re-developed
- Total Ionising Dose (TID)
  - Most space missions are limited to 100 krad dose, and in 180 nm or below, TID protection might be limited to e.g. screening of (commercial) library cells, elimination of certain transistor types
  - Some long duration, deep space missions are in the Mrad domain, requiring mitigation e.g. by special transistor geometries (ELT), guard rings or derating
- Single Event Latch-Up (SEL)
  - Horizontal: mitigation in layout, e.g. guard rings
  - Vertical: thickness of the epitaxial layer, deep n-well
- Single Event Effects (SEE) by Transient and Upset (SET, SEU)
  - Spatial or temporal redundancy
  - Mitigation by design of library cells or in logic design → see below

Roland Weigand (ESA)

ATLAS Silicon detectors upgrade

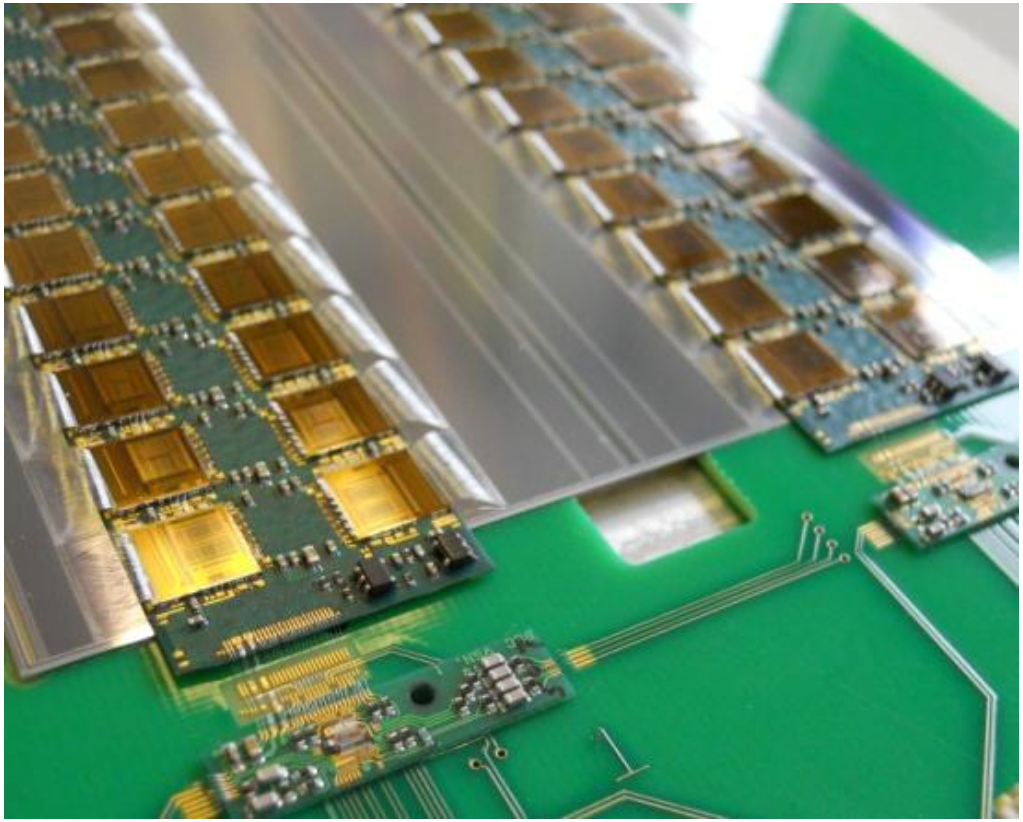
Ashley Greenall (U Liverpool)

Design and Performance of Single-Sided Modules within an Integrated Stave Assembly for the ATLAS Tracker Barrel Upgrade

Ashley Greenall
The University of Liverpool

Silicon strips !

Silicon strips for the ATLAS upgrade



- Introduction to the Stave concept
- Stave flex hybrid
  - Assembly & Electrical performance
- Stave module
  - Assembly & Electrical performance
  - First look at multi-module performance
- Summary and outlook

Silicon strips for the ATLAS upgrade

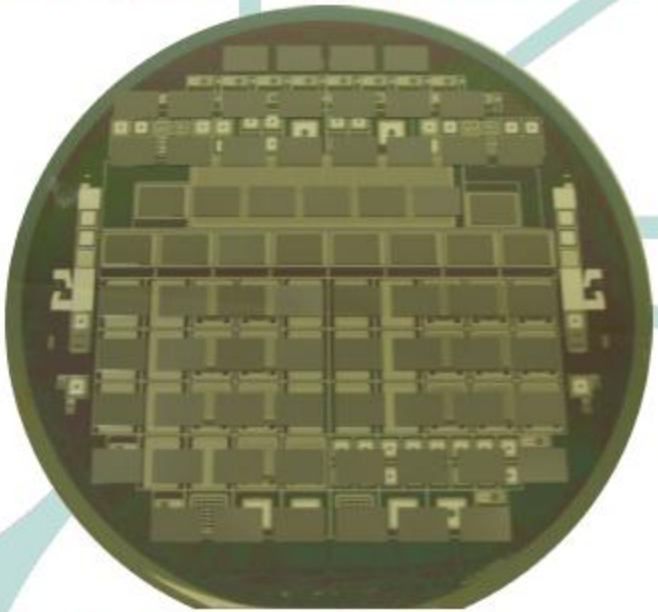
- Have successfully demonstrated the design and build of a substrate-less module
- Issues of yield and volume production being addressed from the outset
- Individually, serially powered modules, have been shown to perform excellently
- First tests of a serially powered multi-module short stave (Stavelet) are very promising

- Stavelet tests are ongoing (with future plans for a DCDC powered variant)
- Intention is to build a module using the new shield-less hybrids (reduced material)
- Longer term, the plan is to build a full size double-sided Stave composed of 24 modules

Ashley Greenall (U Liverpool)

Pixels for the ATLAS upgrade

ICV-SLID interconnection technology for the ATLAS pixel upgrade at SLHC

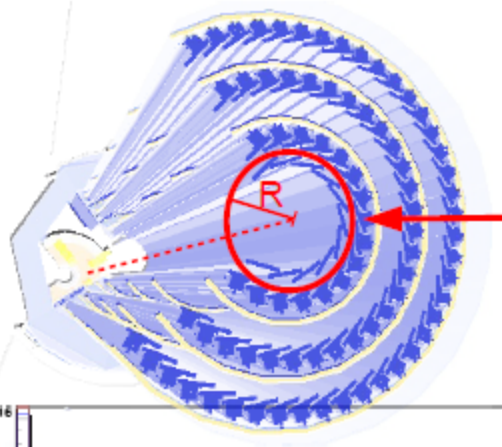


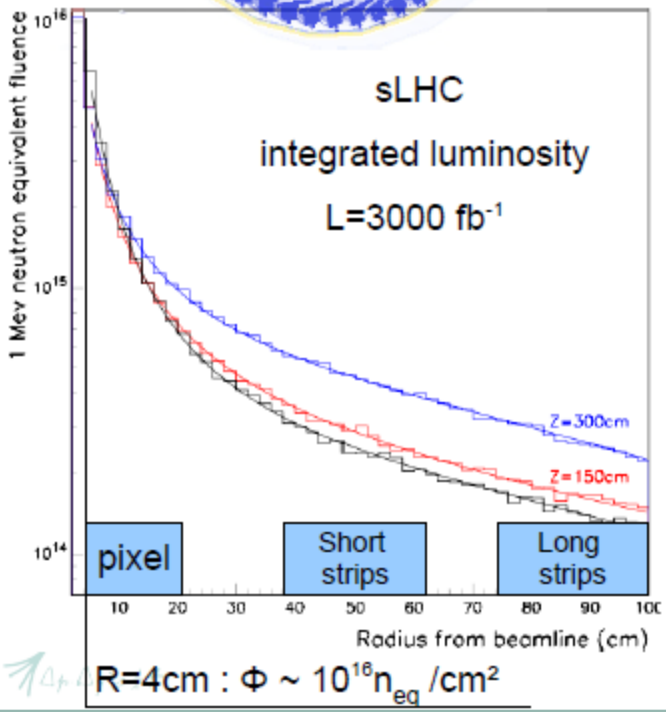
L. Andricek, M. Beimforde, A. Macchiolo,
H.-G. Moser, R. Nisius, R.A. Richter, P. Weigell

Max-Planck-Institut für Physik, München

ATLAS Vertex upgrade (B-Layer)

M. Beimforde: ICV-SLID for the ATLAS pixel upgrade





ATLAS Pixel detector Upgrades

Phase 1 upgrade:

- Surpass LHC design luminosity by ~ 2016
- Insert new innermost pixel layer (b-Layer) **IBL** into the present one. R~3.3cm

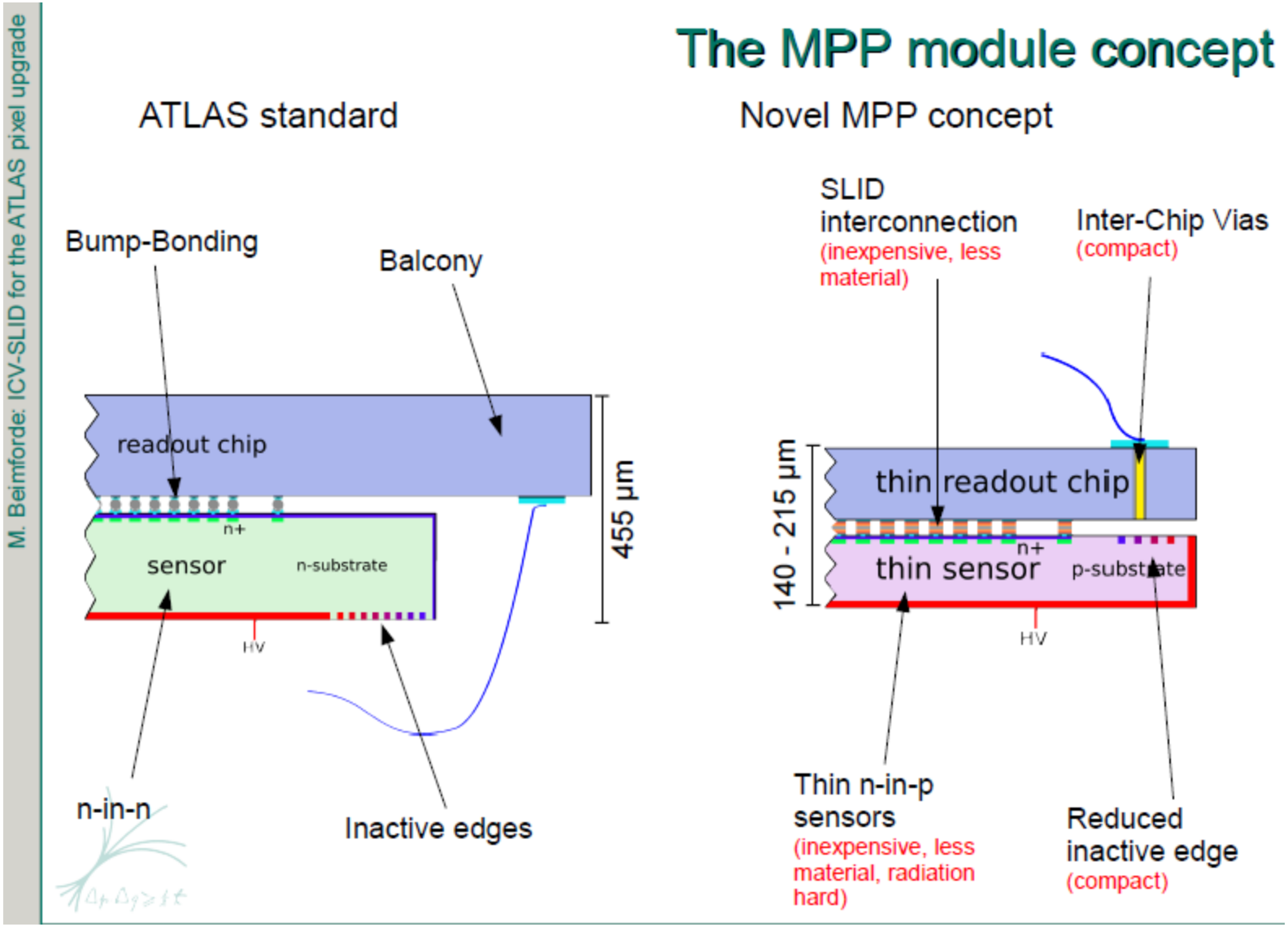
Phase 2 upgrade (Super LHC):

- Plan: (5 -10) x 10^{34}/cm^{2}s → (5 -10)-fold increase
- Completely new pixel detector is needed
- Pixel modules from 3.7cm < R < 20.9cm (current: 5.1cm < R < 12.2cm)
  - Very compact modules needed!
  - Cheap modules wanted!
  - Less multiple scattering (material) desired!

sLHC radiation environment:

- Integrated fluence: $\Phi \sim 10^{16}$ n_{eq} cm^{-2} (scaled to damage of 1 MeV neutrons) after 3000fb^{-1}
- Radiation damage esp. for inner pix. layers
  - Radiation hard modules needed!

Thin Pixel technology

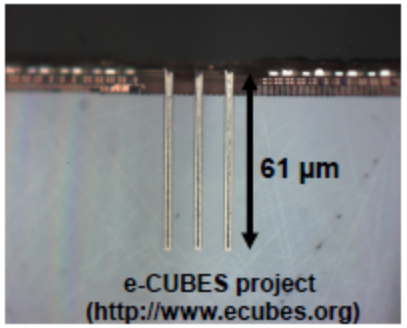


Michael Beimforde (MPI Munich)

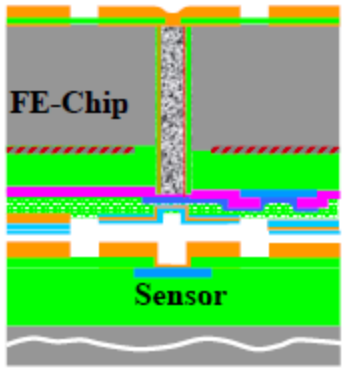
Thin Pixel technology

Inter-Chip Vias

Fraunhofer EMFT

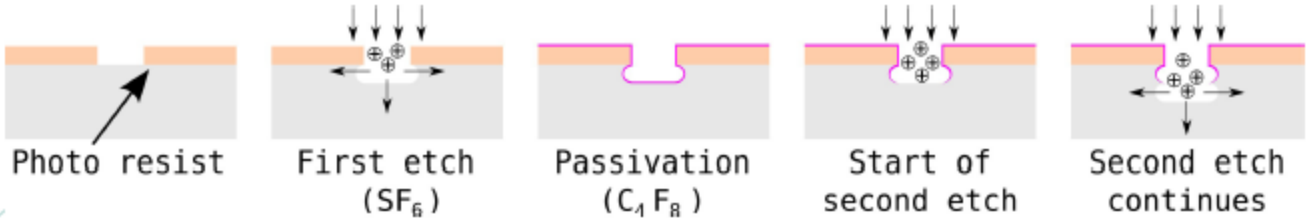


Courtesy: P. Ramm, J. Weber
(Fraunhofer EMFT)



Inter-Chip Vias (ICV):

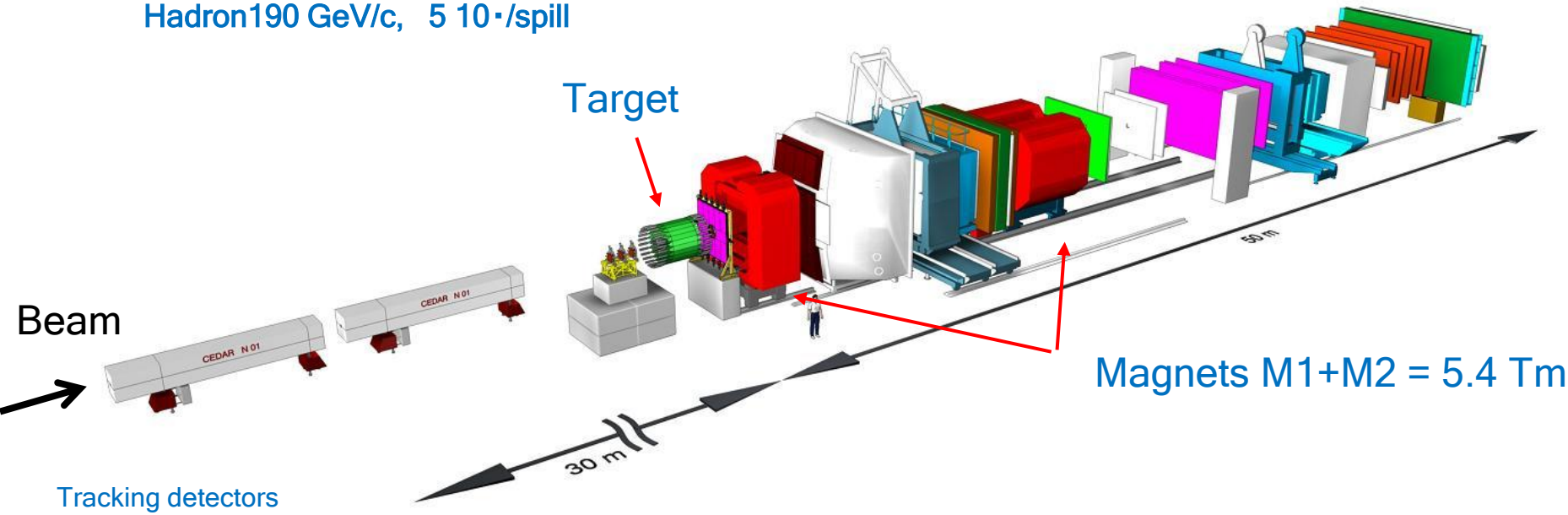
- Allows for vertical signal transport through Si structures
  - Compact pixel modules
- Bosch-process etching and tungsten filling.
- Aspect ratio: 20:1 (3x10x60 µm³)
- Chips thinned to 50 µm
- "Via last approach"
- Active research on 3D multi-tier readout chips is performed (Marseille, Bonn, LBNL with Chartered + Tezzaron)



Triggers

COMPASS spectrometer @SPS CERN

Fixed target experiment , First run 2002
Beam:
Muon 160 GeV/c, 2 10·/spill
Hadron190 GeV/c, 5 10·/spill



Tracking detectors
- Silicon
- Micro-Megas & GEM
- Drift Chambers, Straws

Calorimetry
- ECAL1,2; HCAL1,2 PID
- CEDAR
- RICH
- Muon Wall(filter)

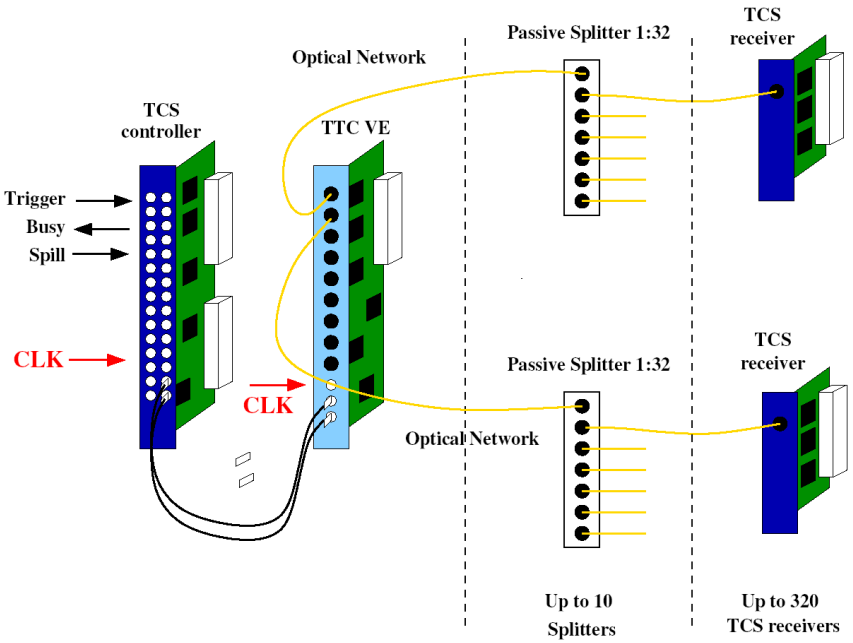
Physics objections:
Nucleon spin structure
Spectroscopy of hadrons

Igor Konorov (TU Munchen)

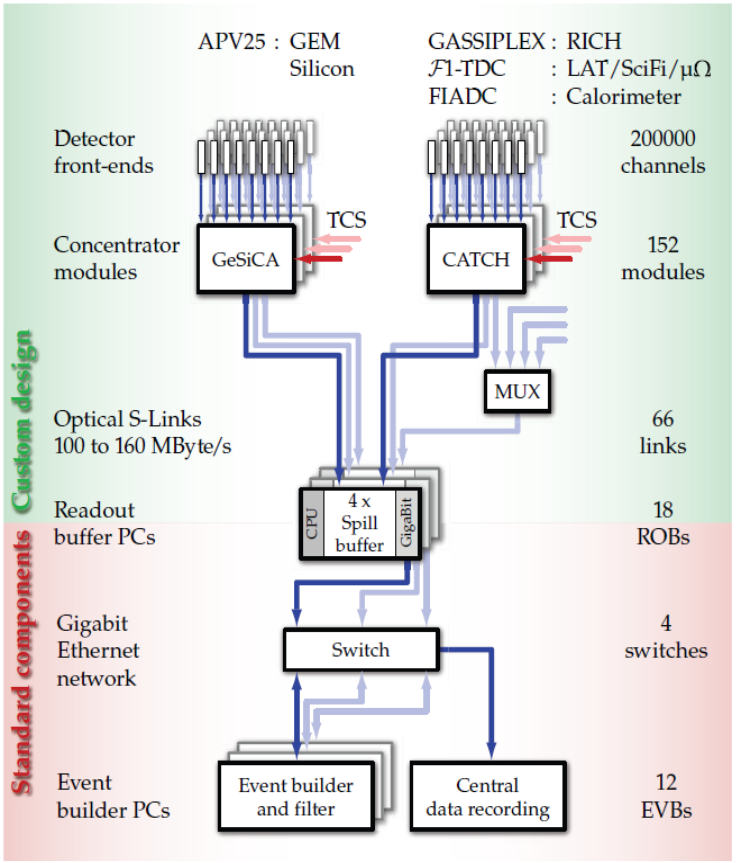
DAQ and Trigger Distribution System

Trigger Control System

- **TCS architecture derived from TTC (LHC)**
- **Built using commercial components**
- **Trigger distributed synchronously with 38.88 MHz clock**



DAQ architecture
DATE(ALICE) DAQ software



Maximum trigger rate: 30kHz

TDC based Trigger Logic in FPGA

Motivation:

Currently COMPASS trigger electronics is based mostly on NIM modules.
Substitute NIM logic with flexible FPGA based electronics

What is the Trigger logic ?

Interconnection of simple logical components: OR, INV, AND

How a Digital Trigger Logic look like:

- Synchronous pipeline architecture – predictable behavior
- Convert analog Timing Information into DIGITs (TDC in FPGA)
- Unified interface : LEMO cable substitutd by FIFO like interface with TDC i
- Library components: NxOR, Nx(N)AND

How to create an FPGA firmware

- Interconnections ⇔ Described in Top level VHDL file
- User creates schematic(net list)
- Software tools generate TOP level VHDL file

Goal: provide a possibility to create a Complex Trigger Logic without a FPGA/VHDL knowledge

Игорь Коноров

Igor Konorov (TU Munchen)

Trigger logic components

- TDC
- Programmable delays
- AND, OR, NAND with programmable coincidence window(GATE) and master signal
- Time calibration – automatic scanning signal timing
- Monitoring
- DAQ interface – no need for splitting signals to TDCs
- Inter module interface for scaling up the system

Software

- GUI for creating trigger logic schematic
- Software for generation VHDL code and project files
- Standard Xilinx tools to be used for implementation
- No special knowledge required for using the system

Igor Konorov (TU Munchen)

Generation top level VHDL file

Input:

- Template file “top_level.vhd”
- Configuration file “trigger_logic.xml”

Java program generate VHDL file

- New signals declaration
- Components instantiation

```
tttt : trigger_logic
    generic map (
        LEVEL => 2,
        SLAVE_NUMBER => 2,
        DELAY_PRO_LEVEL => 10,
        TRIGGER_TYPE => 0
    )
    port map (
        control => control,
        t => t,
        channels_in => channels_in_tttt,
        result => result_tttt
    );
```

```
- <trigger>
    <name>tttt</name>
    <type>AND</type>
  - <signal>
      <name>ts1</name>
      <source>TDC</source>
      <gate>10</gate>
      <notFlag>0</notFlag>
      <master>0</master>
    </signal>
  - <signal>
      <name>ts2</name>
      <source>test</source>
      <gate>10</gate>
      <notFlag>0</notFlag>
    </signal>
  - <signal>
      <name>ts3</name>
      <source>TDC</source>
      <gate>10</gate>
      <notFlag>1</notFlag>
      <master>1</master>
    </signal>
  </trigger>
```

LHC Status and Plans

Physics at LHC

To be solved by LHC !

- The goal of LHC is to complete Standard Model with Higgs boson (to complete electroweak theory)
  - Would explain the particules's masses
    - e^- : 511 keV/c^2, n/p (930 MeV/c^2), μ (105 MeV/c^2), τ (1785 MeV/c^2), Z (91 GeV/c^2), W (80 GeV/c^2)
  - Should be light (less than 200 GeV) following LEP/SLD

- Golden mode at LHC is $H \rightarrow \gamma\gamma$
  - A lot of expectations in EM calorimeters !
  - Other modes have a lot of background, may be not easily under control (strong force)

HEP for pedestrians - TWEPP 2010

Patrick Puzo (LAL Orsay)

Physics at LHC/ILC needs…

From detector point of view

- Very demanding on:
  - hermiticity to improve E_T measurement
  - detector quality (no dead channels)
- Higher granularity requires lower consumption
  - From ATLAS LAr FEB electronics (1W/ch) to ILC needs (100 μW/ch)

Patrick Puzo (LAL Orsay)

HEP for pedestrians - TWEPP 2010

LHC Getting to Nominal (Dates Indicative)

2010	2011	2012	2013	2014	2015	2016
Energy 3.5TeV		Splices, Collimators in IR3	Increase Beam Energy to 7TeV			
β^* of 2m			Decrease β^* to 0.55m			
20% of I_{nom}			Increase k_b to 2808			
Initial			Nominal			
$2\ 10^{32}$			10^{34}			
$1\ fb^{-1}$			$\leq 50\ fb^{-1}/yr$			

Ralph Assmann (CERN)

LHC Overall Strategy >2016 (Dates Indicative)

2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	etc.
														Increase Beam Energy to 16.5 TeV					
				New interaction region ($\beta^*$to 0.2m, luminosity leveling)															
Increase beam brightness																			
Ultimate				HL-LHC										HE-LHC					
2.3 10^{34}				5 10^{34}										2 10^{34}					
≤ 100 fb^{-1}/yr				≤ 200 fb^{-1}/yr										≤ 100 fb^{-1}/yr					

Ralph Assmann (CERN)

(Astérix et les Goths. Texte René Goscinny, Dessins Albert Uderzo, Editeur Hachette)

2035…

Thanks !!!