The DIRC Front-end Electronics Chain for BaBar

P. Bailly, J. Chauveau, L. Del Buono, J.F. Genat, H. Lebbolo, L. Roos, B. Zhang

Laboratoire de Physique Nucléaire et de Hautes Energies, Universités Paris 6 et 7, CNRS/IN2P3, 75252 Paris, France

C. Beigbeder, R. Bernier, D. Breton, T. Caceres, R. Chase, A. Ducorps, A. Hrisoho, P. Imbert, S. Sen, V. Tocut, K. Truong, G. Wormser, F. Zomer

Laboratoire de l'Accélérateur Linéaire, Université Paris-Sud, CNRS/IN2P3, 91405 Orsay, France

G. Bonneaud, F. Dohou, F. Gastaldi, P. Matricon, C. Renard, C. Thiebaux, G. Vasileiadis, M. Verderi

Laboratoire de Physique Nucléaire et de Hautes Energies, Ecole polytechnique, CNRS/IN2P3, 91128 Palaiseau, France

G. Oxoby, J. Va'Vra

Stanford Linear Accelerator Center, Stanford University, PO Box 4349 Stanford CA 94309 USA

D. Warner, R.J. Wilson

Colorado State University, Fort Collins, CO 80523 USA

Abstract

The Detector of Internally Reflected Cerenkov light (DIRC) of the BaBar detector (SLAC Stanford, USA) measures to better than 1ns the arrival time of Cerenkov photoelectrons, detected in a 11,000 phototubes array and their amplitude spectra. It mainly comprises 64-channel DIRC Front-End Boards (DFB) equipped with eight full-custom Analog chips performing zero-cross discrimination with 2 mV threshold and pulse shaping, four full-custom Digital TDC chips for timing measurements with 500 ps binning and a readout logic selecting hits in the trigger window, and DIRC Crate Controller cards (DCC) serializing the data collected from up to 16

Preprint submitted to Elsevier Preprint *10 March 1999*

DFBs onto a 1.2 Gb/s optical link. Extensive test of the pre-production chips have been performed as well as system tests.

1 Introduction

The DIRC [1] is intended to provide particle identification, particularly separate π and K mesons to better than three sigmas for momenta between 0.15 and 4 GeV/c. Cerenkov photons are internally reflected in 144 quartz bars towards 10,752 photomultiplier tubes (PMT). A water tank is used as leverage between the quartz bars ends and the photomultipliers. The Cerenkov angles are deduced from the pattern created on the PMT wall. The momentum is measured in the BaBar Drift Chamber. The noise in the DIRC due to the PMTs themselves is estimated to 1 kHz, the PEP II machine noise is estimated to 30 kHz including a safety factor of ten; for an average $b\bar{b}$ event, 5.7 primary tracks hit the DIRC and produce each 30 photoelectrons with six extra hits from background generated by these tracks. An equivalent number of background photons of the order of 200 is generated by secondary interactions between the event tracks and the detector (mostly Compton scatttering in the quartz). Photomultipliers with a 1 ns time resolution that the Front-End electronics should not degrade significantly, have been chosen, [2]. The Level 1 (L1) trigger is built from Drift Chamber, Calorimeter, and Muons Detector primitives. Its latency is 12 μs, with an uncertainty of one μs. Raw data are stored locally in the TDC chips during the L1 latency. A selection in this chip is performed so that only data in time with the one microsecond trigger window are sent to the DAQ system after reception of the L1 trigger.

2 System Description

A full description of the system is given in [3]. The Front-End electronics, (Figure 1), is installed very close to the detector, in order to avoid cables and get the required single electron sensitivity. CMOS electronics is used wherever possible, housed in 192 DIRC Front-End Boards (DFB). Twelve Front-End crates are linked to the data acquisition system by twelve BaBar standard 1.2 Gbit/s optical fibers. The 1.2 Gbit/s stream is paralleled in the 16-slot crates at 59.5 MHz. Six readout module equipped with Power PC 604 chips process the DIRC data for data-block building, detector calibration, and other purposes. The real-time commands such as Level 1 accept, fast strobes, are dispatched through the BaBar Electronics under control of a Fast Control Timing System housed in the VME DAQ crates.

3 Photomultipliers Electronics

The DIRC PMT base system comprises printed circuit boards equipped with surface mounted components allowing to operate the phototubes around 1.1 kV. A distribution board feeds sixteen PMT channels. The current per PMT base is 150 μA. The High Voltage System, in the electronics house, comprises 56 high voltage channels per sector, sent to the Front-End through twelve 56-way high voltage cables. The voltage can be set between 1 kV and 1.6 kV.

4 DIRC Front-End Board

The DIRC Front-End Board processes 64 PMTs inputs. It houses eight analog chips and their associated level translators, four TDC chips, one 8-bit flash ADC, two digitally controlled calibration generators, multi-event buffers, tests hardware. It is connected to a custom crate backplane, the Protocol Distribution Board (PDB), through one single 96-pins connector interfacing clocks, serial data input and output lines and supplies. The gain of each channel is set on-board with a 5% precision. A unique ground plane is used as a voltage reference for all input signals. Such a grounding scheme, combined with a copper shield housing the analog chips and input circuitry, allows to operate thresholds down to 1 mV, the actual limit reachable on the analog chips test benches. The DFB receives either run-time commands such as L1 accept, readout and calibration strobes, clear multi-event buffers, synchronization, and sub-system commands [8] used for initialization such as calibration control, threshold registers loading, trigger window loading, or hardware tests. The 64 analog outputs are multiplexed towards the single FADC in two possible ways. Either the 64 discriminator outputs are permanently polled by a priority encoder, the selected address is sent back to the relevant analog chip, that outputs the proper analog signal to the FADC, or in calibration mode, an address can be chosen and the corresponding channel output is always sent to the FADC.

5 Analog Chip

The PMT signals are amplified, thresholded and pulse shaped by an 8-channel analog chip [4]. A digital pulse timed with the peak of the input pulse is output by a zero-cross discriminator, as well as a pseudo-gaussian pulse shaped at 80 ns peaking time. This peaking time has been chosen to give to the multiplexing mechanism enough time to take place. A multiplexer selects the analog channel to be digitized on the DFB.

A time resolution better than one nanosecond over a signal amplitude range of 20 is required. In practice, instead using the popular two discriminators technique, one for arming, the other for timing, a single hysteresis comparator is used. The hysteresis is set equal to the threshold. Therefore a leading edge exceeding the threshold fires the discriminator which is cleared when the differentiated input level crosses the ground level. The trailing edge of the output pulse is synchronous with the maximum of the input pulse, it is sent to the TDC chip. The comparator hysteresis is kept constant, the effective threshold being obtained by changing the gain of the input amplifier, corresponding to a threshold between 1 and 10 mV. The dead time after a zero- crossing detection is 80ns.

A pulse shaper peaking at 80ns provides a peak output voltage proportional to the input charge. Analog voltage gain is set between 2.5 and 25. A multiplexer selects the channel to be output towards the ADC. The analog chip is manufactured by AMS (Austria Mikro Systems) using a 1.2 μm 2-poly 2-metal CMOS process. Total power is 200 mW. The chip area is 14 mm^2. It is housed in a 68 pin package. A 2 ns time walk is observed close to the threshold and is reduced to 0.5 ns from 10 to 100 mV. This lead to a timing resolution of 400 ps when averaged over the PMT gaussian amplitude spectrum centered on 20 mV, significantly better than the BaBar experiment requirements.

ec:Analog chip

6 TDC Chip

The TDC chip [5] [6] [7] is a 16-channel TDC with 500 ps binning input buffering and selective readout of the data in time with the trigger. A binning of 500 ps has been chosen, with a full-scale of 32 μs in order to cope with a first level trigger latency of 12 μs, or higher. The selective readout process extracts data in time within a programmable window. Those data are available at any time in an output FIFO. The 0.8 μm CMOS chip is manufactured by ATMEL-ES2. The die size is 36 mm^2, power less than 60 mW at 100 kHz average rate input on all channels, and 60 MHz clock frequency.

The TDC section uses sixteen independent digital delay lines to digitize time with 500 ps binning [5]. A calibration channel allows to tune the chip delays on the 60 MHz reference clock, in order to cope with supply, temperature and process variations. Coarse time is measured with a fast counter common to all channels, providing the 11 most significant bits. Internal buffering [6] is implemented with sixteen independent dual-port channel FIFOs in order to store data before a readout is requested, limiting the detector dead-time to less than 0.1% at 100 kHz input rate. The selective readout process [7]

extracts times from the input FIFOs and builds a time-ordered list stored in an intermediate FIFO during the Level 1 trigger latency. Data beginning to be candidate for a possible incoming trigger are stored into an output FIFO, until they get out of the trigger resolution window. At any time, data in time with an incoming trigger is available for readout.

The average differential linearity on the overall production is 196 ps RMS, including the binning error. The proposed calibration scheme is thus appropriate for the required integration level of 16 channels. Total chip power is less than 60 mW at 100 kHz input rate on all channels. A yield of 90 % is obtained. ec:TDC Chip

7 DIRC Crate Controller

Twelve DIRC Crate Controllers (DCC) interface the Glink fiber optics coming from the six readout modules in the DIRC DAQ VME crate to the DIRC Front-End crates. The DCC comprises mainly the Glink interfaces, and the Monitoring section that manages DIRC Detector environmental controls. It is interfaced to the system using the CAN-bus standard adopted within BaBar. The Monitoring section monitors also the status of the Glink interface, and generates a digital pulse that triggers the light pulser for the DIRC detector calibration. The PDB fans the 60 MHz demultiplexed bit stream from the 1.2 GHz sent through the fiber optics to the fourteen DFBs. Clock jitter measured at the end of a 30 m fiber after clock recovery in the receiver chip is 124 ps RMS in presence of data exchange. The main components of the Glink section are the Glink transmitter/receiver chips from Hewlett-Packard, that perform multiplexing and demultiplexing function, clock recovery, error detection, and link control, and the Optical transmitter/receiver from Finisar. The Monitoring section includes a microcontroller chip, the CAN bus interface, a pulse generator whose delay with respect to a global calibration strobe command is programmable by 500 ps steps, and the sensors for detector slow controls.

8 Results

Extensive tests with the actual DIRC PMTs and a LED light source tuned to generate single photons events have been performed with the full Front-End electronics chain. A threshold of 1 mV can be used without digital to analog crosstalk or unstabilities. Measurements gave resultsbetter than the requirements, both in time accuracy and input rate capability. Cerenkov rings from cosmic rays have been obtained with the detector equipped with the

twelve-crate Front-end electronics (Figure 2).

9 Conclusion

The DIRC Electronics Front-End Chain performs sub-nanosecond timing with single photo-electron over 10,000 channels. It makes use of two custom VLSI chips. The discriminator-shaper chip allows to build single photo-electron response of the photomultipliers during calibration runs. The TDC chip selects data compatible with an incoming Level 1 trigger reducing the dataflow by a factor of 10. Both chips can process input signals up to an 100 kHz average rate. Chips are housed on a 64-channel board read by a Crate Controller connected to the Data Acquisition system using the Glink standard at 1.2 Gbit/s links. This complete electronic chain is housed in a a volume of about $1m^3$ and dissipates less than 5 kW.

References

[1] *BaBar Technical Design Report, SLAC-R-95-457, March 1995*

[2] The DIRC Electronics Group. *BaBar DIRC note 29, DIRC Electronics Requirements, Feb 1996*

[3] The DIRC Electronics Group. *BaBar DIRC note 324, DIRC Electronics, Oct 1996*

[4] J. Ardelean, R.L. Chase, A. Hrisoho, S.Sen, V. Tocut, K. Truong, G. Wormser, "A Discriminator and Shaper Integrated Circuit".

[5] J.F. Genat, High Resolution Time to Digital Converters *Nuclear Instruments and Methods Vol A315, pp411-414, 1992*

[6] P. Bailly, J. Chauveau, J.F. Genat, J.F. Huppert, H. Lebbolo, L. Roos, B. Zhang, A 16-channel Digital TDC chip *This Conference*

[7] B. Zhang, Développement d'un Circuit intégré VLSI assurant Mesure de Temps et Lecture sélective dans l'Electronique Frontale du Détecteur DIRC de l'expé rience BaBar *à* SLAC *Thèse de Doctorat. Université Pierre et Marie Curie. Paris, France. Sept. 1997*

[8] A. Ducorps et al, The DIRC Subsystem Commands *LAL Internal Report 1997*